INTEGRATED CIRCUITS

DATA HANDBOOK

CMOS integrated circuits for clocks and watches

BOOK IC16 1989

Philips Components

PHILIPS

PHILIPS

CMOS INTEGRATED CIRCUITS FOR CLOCKS AND WATCHES

INTRODUCTION

INTRODUCTION

Faselec, a Philips IC subsidary, is one of the most important producers of CMOS integrated circuits for clocks and watches in the world. Situated in Switzerland, the heart of the European clock and watch industry, Faselec benefits to a large degree from this unique industrial environment. It is therefore not surprising, that Faselec was one of the first semiconductor companies to apply the silicon gate CMOS (complementary metal oxide semiconductor) technology in the production of clock and watch circuits and was the first company to offer an SO package (mini-pack) back in the seventies.

Facelec maintains its position at the forefront of the clock and watch IC industry, being the first company to offer the EEPROMs (Electrically Erasable Programmable Read Only Memories), with operating voltages as low as 1,1 V, for frequency adjustment. This latest development enables the industry to find better technical and cost effective solutions for their products.

To enable the clock and watch industry to maintain its world-renowned quality image, Faselec has implemented a Company-Wide Quality Improvement (CWQI) program. This CWQI program, involving every employee of Faselec, features a continuous improvement of customer service and product quality. This commitment to quality has lead to us being able to set our standard at zero defects and now enables us to offer our customers a zero defects warranty. The warranty means that if he finds a single device which does not conform to the published specification, the customer can return the complete lot for rescreening or replacement. Faselec is the first company in the world to offer the clock and watch industry a zero defects warranty.

At Faselec quality is something that dominates all phases of manufacture. Quality is built into the product by the conscious use of advanced technological aids and a continuous monitoring of all process steps through in-line quality controls. Additionally a stringent incoming inspection of all materials used assures an end-product with an inherently high quality level.

All products are 100% tested against published specifications, any device not conforming to the specifications is rejected. Conformity of each lot to the published specifications is double-checked by our Quality department, which is independent from production.

The dedication of the highly-qualified personnel and the large amount of know-how accumulated over the years, backed by constant efforts in developing new process and packaging technology as well as new products, makes Faselec the preferred source for your clock and watch circuits.

SELECTION GUIDE

Functional index

Numerical index

Maintenance type list

FUNCTIONAL INDEX

Analogue watch circuits: 32 kHz

type number	output cycle time	pulse duration	current consumption		EEPROM	comments	page no.
			typ.	max.			
PCA1260	1 s	7.8 ms	150 nA	250 nA	no	end-of-life battery detector and adaptive motor control	27
PCA1261	1 s	7.8 ms	150 nA	250 nA	no	adaptive motor control without end-of-life detector	27
PCA1460	1 s	7.8 ms	170 nA	260 nA	yes	PCA146X series have: EEPROM for frequency trimming, adjustment accuracy ± 1 x 10^{-6} lithium battery voltage level detection (except PCA1464, PCA1465 and PCA1468); battery end-of-life indication (except PCA1461, PCA1464 PCA1465, PCA1466, PCA1467); adaptive motor pulse control	39
PCA1461	1 s	7.8 ms	170 nA	260 nA	yes		39
PCA1462	1 s	5.8 ms	170 nA	260 nA	yes		39
PCA1463	1 s	3.9 ms	170 nA	260 nA	yes		39
PCA1464	1 s	3.9 ms	170 nA	260 nA	yes		39
PCA1465	1 s	5.8 ms	170 nA	260 nA	yes		39
PCA1466	5 s	5.8 ms	170 nA	260 nA	no		39
PCA1467	1 s	7.8 ms	170 nA	260 nA	yes		39
PCA1468	1 s	7.8 ms	170 nA	260 nA	no		39
PCA1481	1 s	7.8 ms	170 nA	260 nA	yes	PCA148X series have: EEPROM for frequency trimming, adjustment accuracy ± 1 x 10^{-6}; battery end-of-life indication; adaptive motor pulse control	53
PCA1482	1 s	5.8 ms	170 nA	260 nA	yes		53

Analogue watch circuits: 32 kHz (continued)

type number	output cycle time	pulse duration	current consumption		EEPROM	comments	page no.
			typ.	max.			
PCA1601	1 s	7.8 ms	170 nA	260 nA	yes	PCA16XX series have: EEPROM for frequency trimming, adjustment accuracy ± 1 x 10^{-6} silver oxide battery voltage level detection; battery end-of-life indicator	83
PCA1602	1 s	7.8 ms	170 nA	260 nA	yes	75% chopped pulse version	83
PCA1605	20 s	4.8 ms	170 nA	260 nA	yes		83
PCA1606	10 s	6.8 ms	170 nA	260 nA	yes		83
PCA1609	1 s	5.8 ms	170 nA	260 nA	yes		83
PCA1671	1 s	7.8 ms	170 nA	260 nA	no	PCA167X series have: trimming adjustment; operate using silver oxide battery, except PCA1672	93
PCA1672	1 s	7.8 ms	200 nA	350 nA*	no	56% chopped pulse version (1 kHz), operates from a 3 V lithium battery	93
PCA1674	5 s	7.8 ms	170 nA	260 nA	no		93
PCA1678	20 s	5.8 ms	170 nA	260 nA	no		93

Analogue clock circuits: 32 kHz

type number	output cycle time	pulse duration	current consumption		EEPROM	comments	page no.
			typ.	max.			
PCA1532	1 s	23.4 ms	2 μA	5 μA	no		67
PCA1534	1 s	46.8 ms	2 μA	5 μA	no		67

*At 3.5 V.

Analogue alarm clock circuits: 32 kHz quartz crystal

type number	output cycle time	pulse duration	current consumption		EEPROM	comments	page no.
			typ.	max.			
PCA1593	1 s	31.25 ms	1.5 μA	5 μA	yes	PCA159X series have: EEPROM for frequency trimming; 64 steps 2 kHz alarm output; alarm output of PCA1593, PCA1594 and PCA1596 is shown in Fig.1; alarm output of PCA1595 and PCA1597 is shown in Fig.2	73
PCA1594	1 s	46.8 ms	1.5 μA	5 μA	yes		73
PCA1595	1 s	46.8 ms	1.5 μA	5 μA	yes		73
PCA1596	1 s	15.6 ms	1.5 μA	5 μA	yes		73
PCA1597	4 s	15.6 ms	1.5 μA	5 μA	yes		73

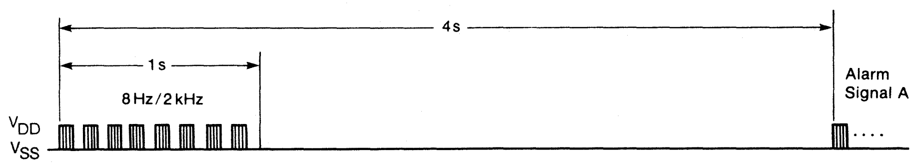


Fig.1 Alarm output diagram A.

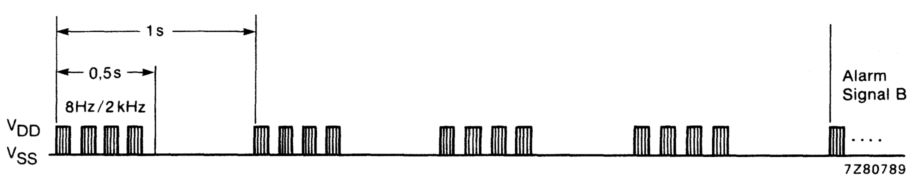


Fig.2 Alarm output diagram B.

Digital car clock circuits: 4.19 MHz quartz crystal

type number	digits	functions: 12 hours mode	24 hours mode	AM/PM annunciator	hours	minutes	direct drive	duplex drive	internal voltage regulator	EEPROM	typical supply current µA	comments	page no.
PCF1171C	4	●	●		●	●	●		●		400		99
PCF1172C	3.5	●		●	●	●	●		●		400		105
PCF1174C	4	●	●	●	●	●	●		●	●	900 to 1500	EEPROM for frequency trimming and internal voltage regulation for LCD	111
PCF1175C	4	●	●	●	●	●		●	●	●	900 to 1500	EEPROM for frequency trimming and internal voltage regulation for LCD	119
PCF1178C	4	●	●	●	●	●		●	●	●	900 to 1500	EEPROM for frequency trimming and internal voltage regulation for LCD	129

NUMERICAL INDEX

type	description	page no.
PCA1260	32 kHz watch circuit with adaptive motor pulse width; bipolar motor; t_T = 1 s; t_p = 7.8 ms; end-of-life detector	27
PCA1261	32 kHz watch circuit with adaptive motor pulse width; bipolar motor; t_T = 1 s; t_p = 7.8 ms	27
PCA1460	32 kHz watch circuit with adaptive motor pulse; EEPROM; bipolar motor; lithium battery voltage level detection; battery end-of-life detection; t_T = 1 s; t_p = 7.8 ms	39
PCA1461	32 kHz watch circuit with adaptive motor pulse; EEPROM; bipolar motor; lithium battery voltage level detection; t_T = 1 s; t_p = 7.8 ms	39
PCA1462	32 kHz watch circuit with adaptive motor pulse; EEPROM; bipolar motor; lithium battery voltage level detection; battery end-of-life detection; t_T = 1 s; t_p = 5.8 ms	39
PCA1463	32 kHz watch circuit with adaptive motor pulse; EEPROM; bipolar motor; lithium battery voltage level detection; battery end-of-life detection; t_T = 1 s; t_p = 3.9 ms	39
PCA1464	32 kHz watch circuit with adaptive motor pulse; EEPROM; bipolar motor; t_T = 1 s; t_p = 3.9 ms	39
PCA1465	32 kHz watch circuit with adaptive motor pulse; EEPROM; bipolar motor; t_T = 1 s; t_p = 5.8 ms	39
PCA1466	32 kHz watch circuit with adaptive motor pulse; bipolar motor; lithium battery voltage level detection; t_T = 5 s; t_p = 5.8 ms	39
PCA1467	32 kHz watch circuit with adaptive motor pulse; EEPROM; bipolar motor; lithium battery voltage levels detection; t_T = 1 s; t_p = 7.8 ms	39
PCA1468	32 kHz watch circuit with adaptive motor pulse; bipolar motor; battery end-of-life detection; t_T = 1 s; t_p = 7.8 ms	39
PCA1481	32 kHz watch circuit with adaptive motor pulse; EEPROM; battery end-of-life detection; t_T = 1 s; t_p = 7.81 ms	53
PCA1482	32 kHz watch circuit with adaptive motor pulse; EEPROM; battery end-of-life detection; t_T = 1 s; t_p = 5.86 ms	53
PCA1532	32 kHz clock circuit; bipolar motor; t_T = 1 s; t_p = 23.4 ms	67
PCA1534	32 kHz clock circuit; bipolar motor; t_T = 1 s; t_p = 46.8 ms	67

type	description	page no.
PCA1593	32 kHz alarm clock circuit with frequency adjustment; EEPROM; bipolar motor; alarm signal repeated every 1 s; t_T = 1 s; t_p = 31.25 ms	73
PCA1594	32 kHz alarm clock circuit with frequency adjustment; EEPROM; bipolar motor; alarm signal repeated every 4 s; t_T = 1 s; t_p = 46.8 ms	73
PCA1595	32 kHz alarm clock circuit with frequency adjustment; EEPROM; bipolar motor; alarm signal repeated every 1 s; t_T = 1 s; t_p = 46.8 ms	73
PCA1596	32 kHz alarm clock circuit with frequency adjustment; EEPROM; bipolar motor; alarm signal repeated every 4 s; t_T = 1 s; t_p = 15.6 ms	73
PCA1597	32 kHz alarm clock circuit with frequency adjustment; EEPROM; bipolar motor; alarm signal repeated every 1 s; t_T = 1 s; t_p = 15.6 ms	73
PCA1601	32 kHz watch circuit with EEPROM; silver oxide battery voltage level detection; t_T = 1 s; t_p = 7.8 ms	83
PCA1602	32 kHz watch circuit with EEPROM; silver oxide battery voltage level detection; 75% chopped version; t_T = 1 s; t_p = 7.8 ms	83
PCA1604	32 kHz watch circuit with EEPROM; silver oxide battery voltage level detection; t_T = 5 s; t_p = 7.8 ms	83
PCA1605	32 kHz watch circuit with EEPROM; silver oxide battery voltage level detection; t_T = 20 s; t_p = 4.8 ms	83
PCA1606	32 kHz watch circuit with EEPROM; silver oxide battery voltage level detection; t_T = 10 s; t_p = 6.8 ms	83
PCA1609	32 kHz watch circuit with EEPROM; silver oxide battery voltage level detection; t_T = 1 s; t_p = 5.8 ms	83
PCA1671	32 kHz watch circuit using a silver oxide or 3 V lithium battery; silver oxide battery; t_T = 1 s; t_p = 7.8 ms	93
PCA1672	32 kHz watch circuit using a silver oxide or 3 V lithium battery; 3 V lithium battery; 75% chopped pulse version; t_T = 1 s; t_p = 7.8 ms	93
PCA1674	32 kHz watch circuit using a silver oxide or 3 V lithium battery; silver oxide battery; t_T = 5 s; t_p = 7.8 ms	93
PCA1678	32 kHz watch circuit using a silver oxide or 3 V lithium battery; silver oxide battery; t_T = 20 s; t_p = 5.8 ms	93
PCF1171C	4.19 MHz digital LCD car clock; 4 digits	99
PCF1172C	4.19 MHz digital LCD car clock; 3½ digits	105
PCF1174C	4.19 MHz 4-digit static-LCD car clock; EEPROM	111
PCF1175C	4.19 MHz 4-digit duplex-LCD car clock; EEPROM	119
PCF1178C	4.19 MHz 4-digit static-LCD car clock; EEPROM; mirrored version of PCF1175; different colon and set frequency	129

MAINTENANCE TYPE LIST

The types listed below are not included in this handbook. Detailed information will be supplied on request.

PCA1200 series (superseded by PCA167X series)

PCA1400 series (superseded by PCA16XX series)

PCA1512

PCA1517

PCA1580 series (superseded by PCA159X series)

PCF1171 (superseded by PCF1171C)

PCF1172 (superseded by PCF1172C)

PCF1174 (superseded by PCF1174C)

PCF1175 (superseded by PCF1175C)

GENERAL

Type designation
Rating systems
Handling MOS devices

PRO ELECTRON TYPE DESIGNATION CODE FOR INTEGRATED CIRCUITS

This type nomenclature applies to semiconductor monolithic, semiconductor multi-chip, thin-film, thick-film and hybrid integrated circuits.

A basic number consists of:

THREE LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST AND SECOND LETTER

1. DIGITAL FAMILY CIRCUITS

   The FIRST TWO LETTERS identify the FAMILY (see note 1).

2. SOLITARY CIRCUITS

   The FIRST LETTER divides the solitary circuits into:

   S : Solitary digital circuits
   T : Analogue circuits
   U : Mixed analogue/digital circuits

   The SECOND LETTER is a serial letter without any further significance except 'H' which stands for hybrid circuits.

3. MICROPROCESSORS

   The FIRST TWO LETTERS identify microprocessors and correlated circuits as follows:

   MA : { Microcomputer / Central processing unit
   MB : Slice processor (see note 2)
   MD : Correlated memories
   ME : Other correlated circuits (interface, clock, peripheral controller, etc.)

4. CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

   The FIRST TWO LETTERS identify the following:

   NH : Hybrid circuits
   NL : Logic circuits
   NM : Memories
   NS : Analogue signal processing, using switched capacitors
   NT : Analogue signal processing, using CTDs
   NX : Imaging devices
   NY : Other correlated circuits

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).
2. By 'slice processor' is meant: a functional slice of microprocessor.

THIRD LETTER

It indicates the operating ambient temperature range.
The letters A to G give information about the temperature:

A : temperature range not specified
B : 0 to + 70 °C
C : –55 to + 125 °C
D : –25 to + 70 °C
E : –25 to + 85 °C
F : –40 to + 85 °C
G : –55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example: the range 0 to + 75 °C can be indicated by 'B' or 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

A VERSION LETTER

Indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack
L : for chip on tape
P : for plastic DIL
Q : for QIL
T : for miniature plastic (mini-pack)
U : for uncased chip

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

C : Cylindrical
D : Dual-in-line (DIL)
E : Power DIL (with external heatsink)
F : Flat (leads on 2 sides)
G : Flat (leads on 4 sides)
K : Diamond (TO-3 family)
M : Multiple-in-line (except Dual-, Triple-, Quadruple-in-line)
Q : Quadruple-in-line (QIL)
R : Power QIL (with external heatsink)
S : Single-in-line
T : Triple-in-line

SECOND LETTER: Material

C : Metal-ceramic
G : Glass-ceramic (cerdip)
M : Metal
P : Plastic

A hyphen precedes the suffix to avoid confusion with a version letter.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.
Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and d.c. lines.

DEVICE DATA

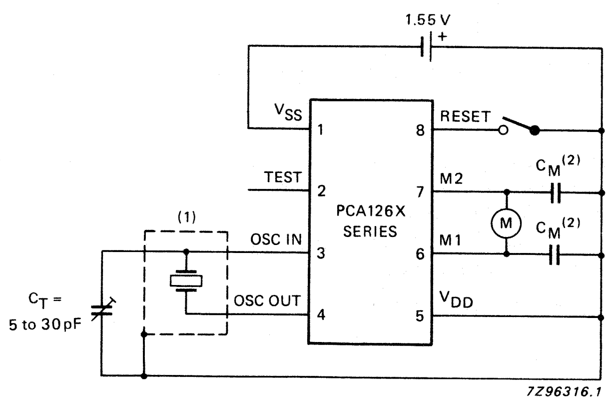
32 kHz WATCH CIRCUIT WITH ADAPTIVE MOTOR PULSE WIDTH

GENERAL DESCRIPTION

The PCA126X series are CMOS integrated circuits specially suited for battery-operated, quartz-crystal-controlled wrist-watches, with a bipolar stepping motor.

Features

- 32 kHz oscillator, amplitude regulated with excellent frequency stability
- High immunity of the oscillator to leakage currents
- Oscillator output capacitor is integrated, only crystal and trimmer required as external components
- Very low current consumption: typically 160 nA
- Output for bipolar stepping motors of different types
- Up to 50% reduction in motor current, compared with conventional circuits, by self adaption of the motor pulse width according to the required torque of the motor
- No loss of motor steps possible because of on-chip detection of the induced motor voltage
- Stop function for accurate timing
- Various test modes for testing the mechanical parts of the watch as well as the IC itself
- Two available types: PCA1260 and PCA1261



(1) Quartz crystal case should be connected to V_{DD}. Stray capacitance and leakage resistance from RESET, M1 or M2 to OSC IN should be less than 0.5 pF or larger than 100 MΩ.

(2) Motor, probe and stray capacitance from M2 or M1 to V_{DD} should be less than C_M = 80 pF for correct operation of the detection circuit.

Fig.1 Typical application circuit diagram.

PACKAGE OUTLINES

PCA126XT: 8-lead micro-flat-pack; plastic (SOT144).
PCA126XU: chip in tray.

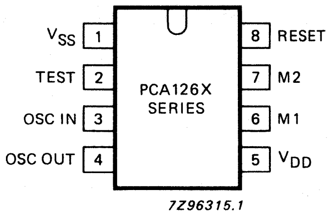


Fig.2 Pinning diagram.

PINNING

1	V_{SS}	ground (0 V)
2	TEST	test input
3	OSC IN	oscillator input
4	OSC OUT	oscillator output
5	V_{DD}	supply voltage
6	M1	motor 1 output
7	M2	motor 2 output
8	RESET	reset input

FUNCTIONAL DESCRIPTION AND TESTING

The motor output delivers pulses of six different widths depending on the torque required to turn the motor (Fig.4). Every motor pulse is followed by a detection phase which monitors the waveform of the induced motor voltage. If a step is missed a correction sequence will be started (Fig.3).

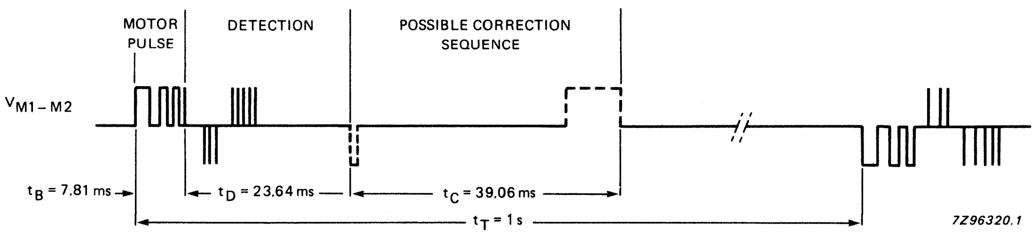


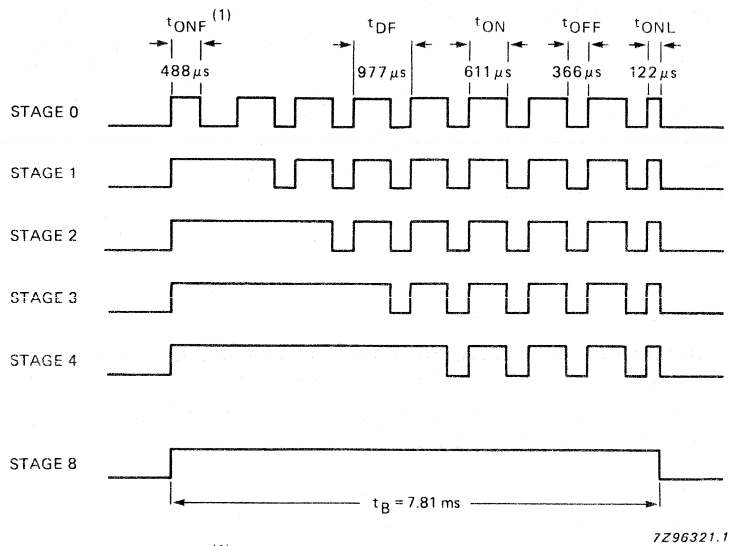
Fig.3 Typical motor output waveform with motor connected.

Motor pulses

The circuit produces motor pulses of six different widths, or stages. Stages 0 to 4 are used in normal operation, stage 8 occurs under the following conditions:

- correction pulse (after a missing step)
- end-of-life pulses (not implemented on PCA1261)
- if stage 4 is not enough to turn the motor

After a RESET the circuit always starts with a 0.



(1) t_{ONF} for stage 0 to 4 = 488 μs + stage x 977 μs

Fig.4 Different forms of motor pulses.

The circuit operates for 64 motor pulses at a fixed stage, if every motor pulse is executed. The next 64 motor pulses are then produced at the next lower stage unless a missing step is detected. If a step is missed a correction sequence is produced and the next 63 motor pulses are increased by one stage.

If motor pulses at stage 4 are not large enough, motor pulses of stage 8 will be produced for a maximum of 63 pulses and no attempt will be made to maintain a low current consumption. After this sequence the circuit starts at stage 0 to be stabilized on as low a stage as possible as fast as possible.

Detection of motor pulses

After a motor pulse, the energy in the motor inductor will be dissipated to measure only the current generated by the induced motor voltage. During the time t_{DI} (dissipation of energy time) all switches shown in Fig.5 are open to reduce the current as fast as possible. The current will now flow through the diodes D3 and D2, or D4 and D1 respectively. Then the first of 46 possible measurement cycles (t_{MC}) starts to measure the induced current.

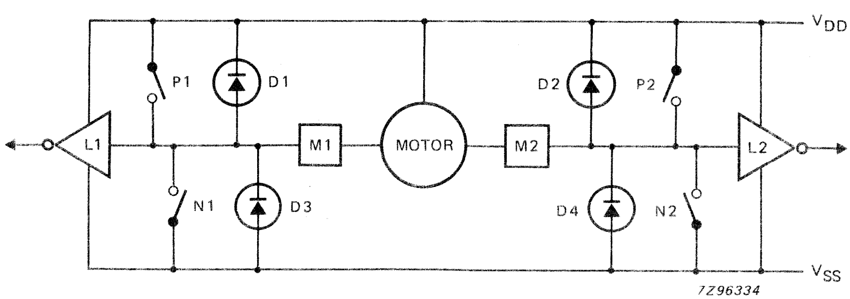


Fig.5 Motor driving and detecting circuit.

Detection criterion (Figs 6 and 7)

	PCA1260	PCA1261
Part 1		
• number of measured positive current polarities after t_{DI}	P = 3	P = 1
Part 2		
• number of measured positive current polarities since the first negative current polarity is detected after part 1 (see Fig.7)	N = 5	N = 2
End-of-life cycle	yes	no

If the opposite polarity is measured in one part, the internal counter is reset, so the results of all measurements in this part are ignored.

The waveform of the induced current must enable all these measurements within the time t_D after the end of a positive motor pulse in order to be accepted as a waveform of an executed motor pulse.

If the detection criterion is satisfied earlier, a measurement cycle will not be started and the switches P1 and P2 stay closed, the motor is switched to V_{DD}.

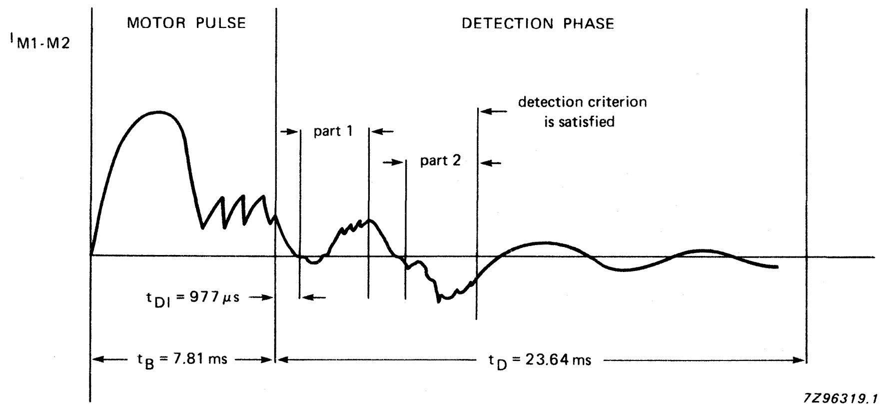


Fig.6 Typical current waveform of a successfully executed motor pulse.

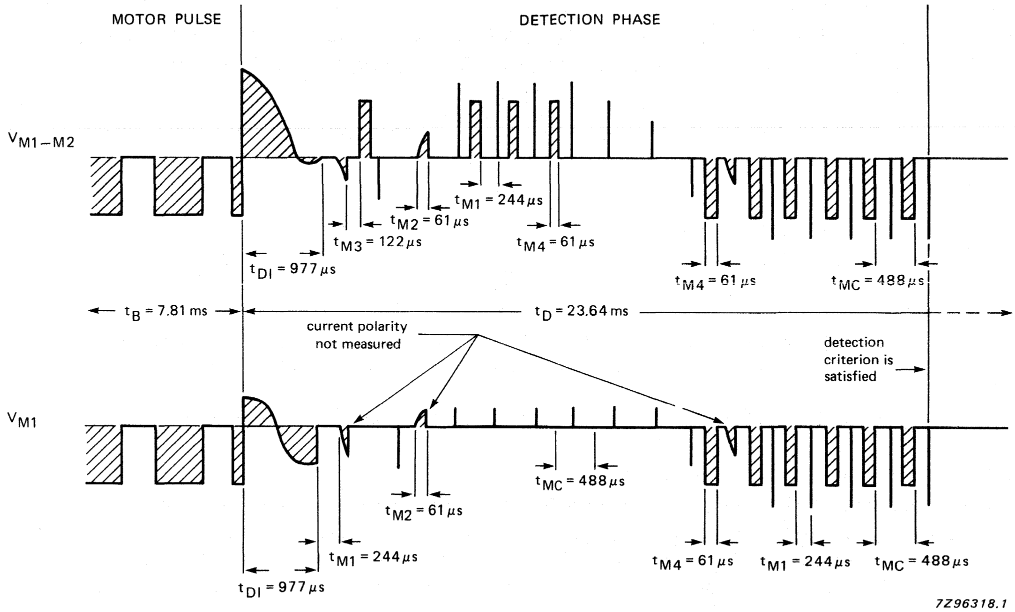


Fig.7 Detection phase of the current waveform in Fig.6.

Every measurement cycle (t_{MC}) has 4 phases, they are as follows:

Phase 1: (t_{M1}) During t_{M1} the switches P1 and P2 are closed in order to switch the motor to V_{DD}, so the induced current flows unaffected through the motor inductance.

Phase 2: (t_{M2}) Measures the induced current. During a maximum time t_{M2} all switches are open until a change is sensed by one of the level detectors (L1, L2). The motor is shorted to V_{DD}. Depending on the direction of the interrupted current flow either:

- the current flows through diodes D3 and D2, causing the voltage at M1 to decrease in relation to M2;
- the current flows through diodes D4 and D1, causing the voltage at M2 to decrease in relation to M1.

A successfully detected current polarity is normally characterized by a short pulse of 0.5 to 10 µs with a voltage up to ± 2.1 V, failed polarity detection by the maximum pulse width of 61 µs and a voltage of ± 0.5 V (see Fig.7).

Phase 3: (t_{M3}) The switches P1 and P2 remain closed for the time t_{M3}. If the circuit does not detect the expected polarity, phase 3 is lengthened by the time t_{M4} and phase 4 is omitted.

Phase 4: (t_{M4}) A pulse of time t_{M4} occurs to reduce the induced current. Therefore P2 and P1 are opened and N1 and N2 are closed.

Detection and pulse width control will be switched off, when battery voltage is below the end-of-life voltage (V_{EOL}) or if stage 4 is not sufficient to turn the motor.

Correction sequence (Fig.8)

If a missing step is detected, a correction sequence is produced. This consists of a small pulse (t_{C1}) which gives the motor a defined position and after 31,25 ms a pulse of stage 8 (t_{C2}) to turn the motor.

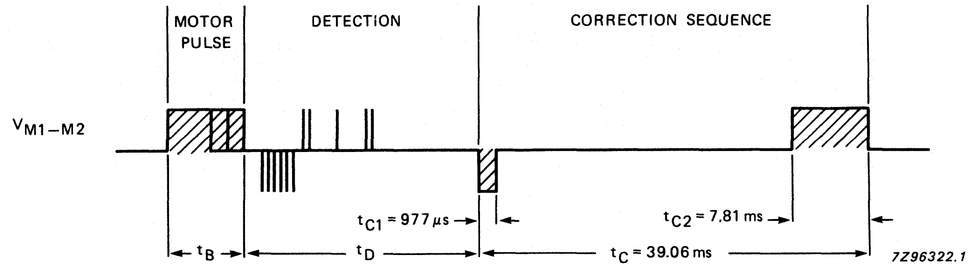


Fig.8 Correction sequence after a missing motor step with motor connected.

End-of-life (only applicable to PCA1260).

The supply voltage V_{DD} is compared with the internal voltage reference V_{EOL} every 4 s. If the end-of-life of the battery is detected ($V_{DD} < V_{EOL}$), detection and pulse width control will be switched off and the waveforms produced will be of stage 8. In addition the pulses are produced in bursts of 4 pulses every 4 seconds to indicate this condition. After a motor stop the first detection of end-of-life will be made a half a second later.

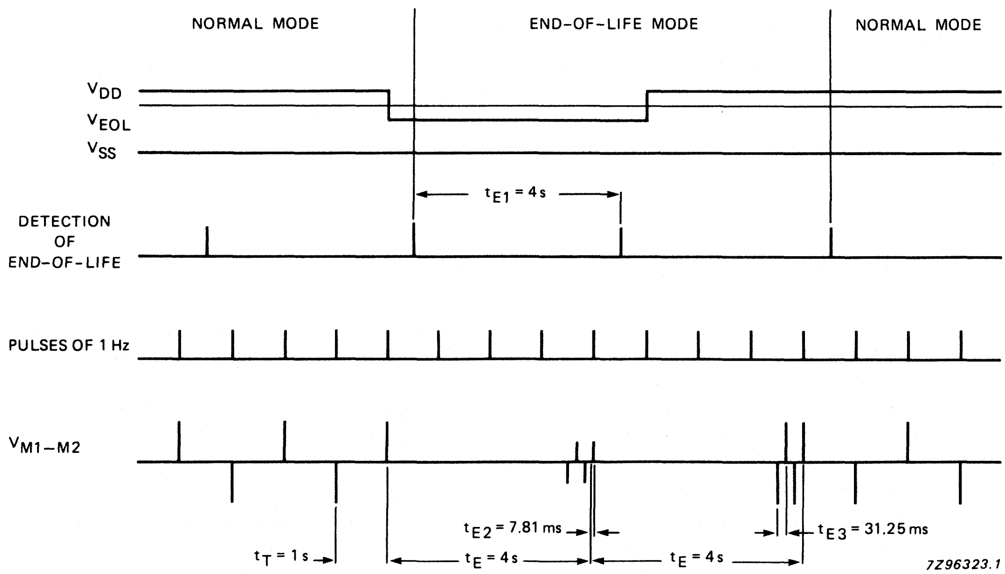


Fig.9 Motor pulses in end-of-life mode.

Customer testing

An output frequency of 32 Hz is provided at RESET (pin 8) to be used for testing and tuning the oscillator.

Connecting the RESET to V_{DD} stops the motor pulses and sets the motor pulse width for the next available motor pulse to stage 0; then, the motor pulses adapt according to the required torque. The RESET input has a built-in delay of 15.7 to 78.1 ms to prevent an accidential motor stop caused by shock or contact bounce. After RESET is activated the first pulse appears with a time delay of 1 s.

Connecting RESET to V_{SS} activates the test mode. With $V_{DD} > V_{EOL}$ motor pulse of stage 8 in a period t_{T1} are produced (Test 1).

If V_{DD} is less than V_{EOL} motor pulses of stage 8 but with a period of t_{T2} are produced (Test 2). In Test 1 and Test 2 the end-of-life detector operates every 7.81 ms.

If V_{DD} is increased again to a voltage higher than V_{EOL}, normal function takes place but the motor pulse period is t_{T3} = 125 ms instead of 1 s (Test 3). In addition the level of the pulse width is reduced every second.

Test and reset mode are terminated by disconnecting the RESET pin.

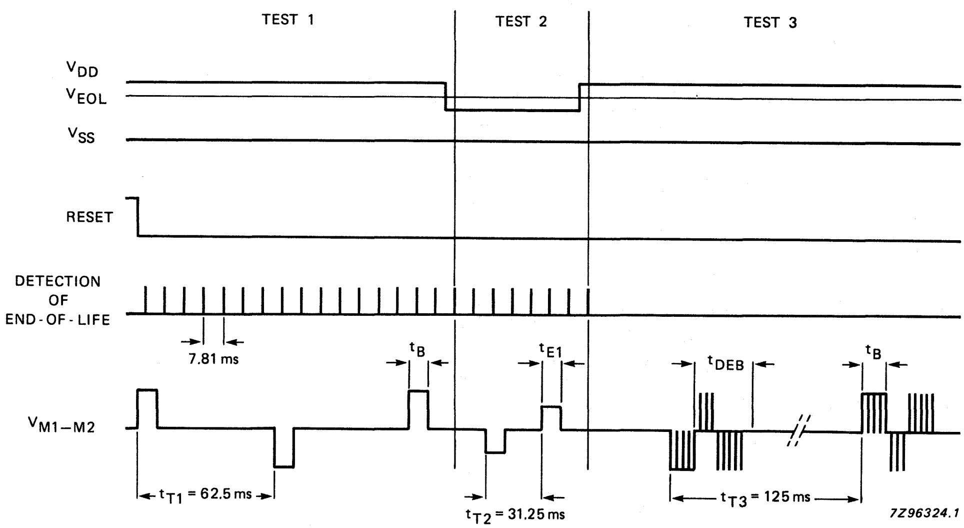


Fig.10 Output pulses in test modes with RESET at V_{SS}.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (V_{SS} = 0 V); note 1	V_{DD}	−1.8 to + 5 V
All input voltages; note 2	V_I	V_{SS} to V_{DD} V
Output short-curcuit duration		indefinite
Operating ambient temperature range	T_{amb}	−10 to + 60 °C
Storage temperature range	T_{stg}	−30 to + 100 °C

Notes

1. Connecting the battery with reversed polarity does not destroy the circuit, but in this condition a large current flows, which will rapidly discharge the battery.
2. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 1.55 V; V_{SS} = 0 V; C_T = 12 pF; f_{osc} = 32.768 kHz; T_{amb} = 25 °C; crystal: R_S = 20 kΩ; C_1 = 2 to 3 fF; C_L = 8 to 10 pF; C_o = 1 to 3 pF; unless otherwise specified.
Immunity against parasitic impedance = 20 MΩ from one pin to an adjacent pin.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD1}	1.2	1.55	2.0	V
Supply voltage	T_{amb} = −10 to + 60 °C	V_{DD2}	1.2	−	1.8	V
Supply voltage	transient within 1.2 V and 2 V	ΔV_{DD}	−	−	0.45	V
Supply current	between motor pulses	I_{DD1}	−	150	250	nA
Supply current	stop mode; pin 8 connected to V_{DD}	I_{DD2}	−	160	280	nA
Supply current	T_{amb} = −10 to + 60 °C	I_{DD3}	−	−	400	nA
Motor output						
Saturation voltage Σ (P + N)	R_M = 2 kΩ	V_{sat}	−	100	150	mV
Saturation voltage Σ (P + N)	R_M = 2 kΩ T_{amb} = −20 to + 60 °C	V_{sat}	−	−	200	mV
Output short-short-circuit impedance	between motor pulses $I_{transistor} < 1$ mA	R_{os}	−	200	300	Ω

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Starting voltage		$V_{OSC\ ST}$	1.2	–	–	V
Transconductance	$V_{i(p-p)} \leq 50$ mV	g_m	6	15	–	μS
Start-up time		t_{osc}	–	1	5	s
Frequency stability	$\Delta V_{DD} = 100$ mV	$\Delta f/f$	–	0.05×10^{-6}	0.3×10^{-6}	
Frequency tolerance	device-to-device	$\Delta f/f$	–	$\pm 3 \times 10^{-6}$	$\pm 10 \times 10^{-6}$	
Input capacitance		C_i	–	4	–	pF
Output capacitance	$V_{i(p-p)} \leq 50$ mV	C_o	19	24	29	pF
End-of-life detection						
Threshold voltage						
PCA1260	normal and test mode	V_{EOL}	1.20	1.30	1.44	V
PCA1261	test mode only	V_{EOL}	1.20	1.30	1.49	V
Hysteresis of threshold		ΔV_{EOL}	–	10	–	mV
Temperature coefficient		$\frac{\Delta V_{EOL}}{dT}$	–	+ 1.0	–	mV/K
Reset						
Output frequency		f_o	–	32	–	Hz
Output voltage swing	R = 1 MΩ, C = 10 pF	ΔV_o	1.4	–	–	V
Edge time	R = 1 MΩ, C = 10 pF	t_e	–	1	–	μs
Peak input current	note 1	I_{im}	–	320	–	nA
Average input current		$I_{i(av)}$	–	10	–	nA

Note to the characteristics

1. Duty factor is 1:32 and RESET = V_{DD} or V_{SS}.

TIMING PARAMETERS

section	remark	symbol	value	option	unit
Motor pulse Figs 3 and 4	cycle for motor pulse	t_T	1		s
	motor pulse width	t_B	7.81		ms
	duty factor	t_{DF}	977		μs
	duty factor on	t_{ON}	611		μs
	duty factor off	t_{OFF}	366		μs
	first duty factor on	t_{ONF}	488		μs
	last duty factor on	t_{ONL}	122		μs
Detection Fig.7	detection sequence	t_D	23.64		ms
	dissipation of energy	t_{DI}	977	1954	μs
	measured cycle	t_{MC}	488		μs
	phase 1	t_{M1}	244		μs
	phase 2 (measure window)	t_{M2}	61		μs
	phase 3	t_{M3}	122		μs
	phase 4	t_{M4}	61		μs
	positive current:				
	PCA1260	P	3	1 to 7	
	PCA1261	P	1		
	negative current:				
	PCA1260	N	5	1 to 7	
	PCA1261	N	2		
Correction sequence Fig.8	correction sequence	t_C	39.06		ms
	small pulse width	t_{C1}	977		μs
	large pulse width	t_{C2}	7.81		ms
End-of-life Fig.9	EOL sequence	t_E	4		s
	detection of EOL	t_{E1}	4		s
	motor pulse width	t_{E2}	7.81		ms
	time between pulses	t_{E3}	31.25		ms
Testing Fig.10	cycles for motor				
	pulses in: Test 1	t_{T1}	62.5		ms
	Test 2	t_{T2}	31.25		ms
	Test 3	t_{T3}	125		ms
	debounce time for RESET = V_{DD}	t_{DEB}	15.7 to 78.1		ms

CHIP DIMENSIONS AND BONDING PAD LOCATIONS

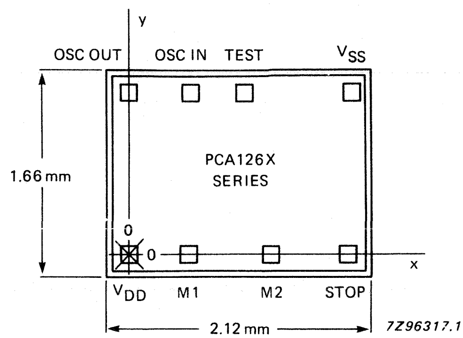


Fig.11 Bonding pad locations.

Bonding pad dimensions 110 μm x 110 μm
Chip area = 3.41 mm^2

Table 1 Bonding pad location (dimensions in μm)
All x, y co-ordinates are referenced to the bottom left pad (V_{DD}), see Fig.11.

pad	x	y
V_{SS}	1795	1290
TEST	925	1290
OSC IN	500	1290
OSC OUT	0	1290
V_{DD}	0	0
M2	485	0
M1	1145	0
STOP	1765	0
chip corner max. value	−160	−160

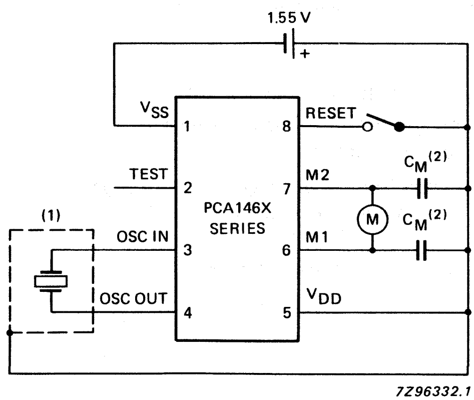
32 kHz WATCH CIRCUIT WITH ADAPTIVE MOTOR PULSE

GENERAL DESCRIPTION

The PCA146X series are CMOS integrated circuits specially suited for battery-operated, quartz-crystal-controlled wrist-watches, with a bipolar stepping motor.

Features

- 32 kHz oscillator, amplitude regulated with excellent frequency stability
- High immunity of the oscillator to leakage currents
- Timekeeping adjustment electrically programmable and reprogrammable (via EEPROM)
- A quartz crystal is the only external component required
- Very low current consumption: typically 170 nA
- Output for bipolar stepping motors of different types
- Up to 50% reduction in motor current compared with conventional circuits, by self adaption of the motor pulse width according to the required torque of the motor
- No loss of motor steps possible because of on-chip detection of the induced motor voltage
- Detector for lithium or silver oxide battery voltage levels
- Indication for battery end-of-life
- Stop function for accurate timing
- Power-on reset for fast testing
- Various test modes for testing the mechanical parts of the watch as well as the IC itself



(1) Quartz crystal case should be connected to V_{DD}. Stray capacitance and leakage resistance from RESET, M1 or M2 to OSC IN should be less than 0.5 pF or larger than 20 MΩ.
(2) Motor, probe and stray capacitance from M2 or M1 to V_{DD} or V_{SS} should be less than C_M = 80 pF for correct operation of the detection circuit. Driving the motor at its minimum energy, probe and stray capacitance must be avoided.

Fig.1 Typical application circuit diagram.

PACKAGE OUTLINES

PCA146XT: 8-lead micro-flat-pack; plastic (SOT144).
PCA146XU: chip in tray.

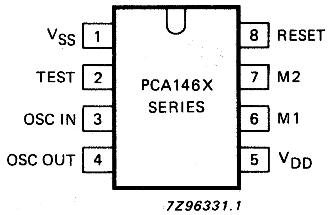


Fig.2 Pinning diagram.

PINNING

1	V_{SS}	ground (0 V)
2	TEST	test input
3	OSC IN	oscillator input
4	OSC OUT	oscillator output
5	V_{DD}	supply voltage
6	M1	motor 1 output
7	M2	motor 2 output
8	RESET	reset input

FUNCTIONAL DESCRIPTION AND TESTING

The motor output delivers pulses of six different stages depending on the torque required to turn the motor (Fig.4). Every motor pulse is followed by a detection phase which monitors the waveform of the induced motor voltage. When a step is missed a correction sequence will be started (Fig.3).

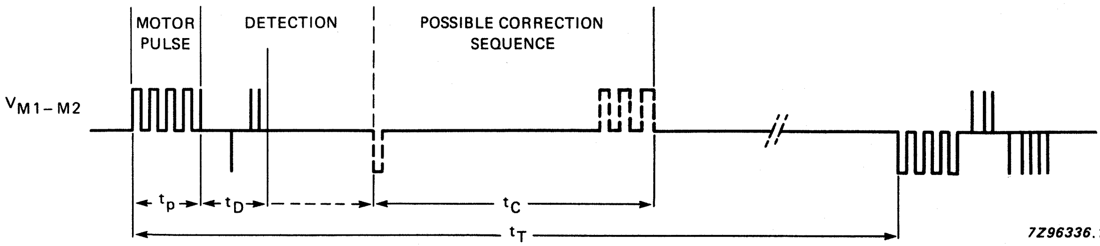


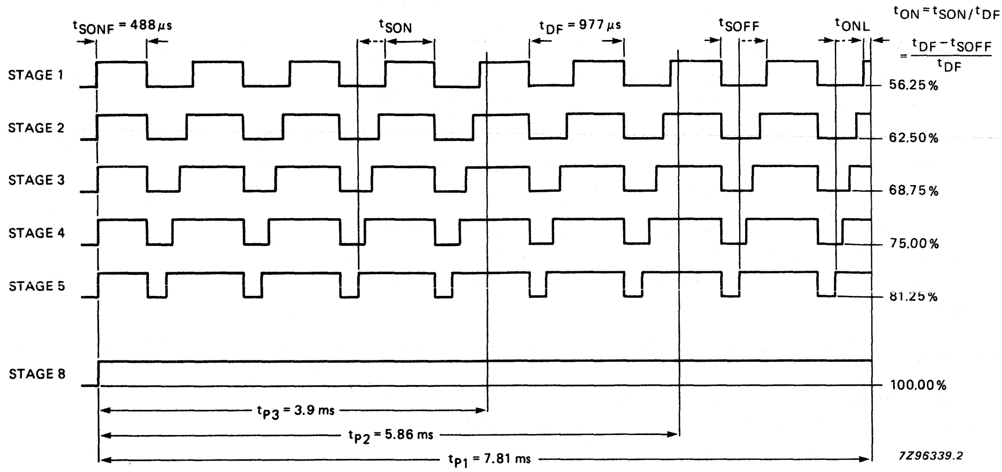
Fig.3 Possible motor output waveform in normal operation with motor connected.

Motor pulses

The circuit produces motor pulses of six different stages (stage 1 to 5, stage 8). Each stage has two independent modes; silver oxide and lithium. The voltage level of V_{DD} determines which mode is selected (see section 'Voltage level detector').

Stages 1 to 5 (both modes) are used in normal operation, stage 8 occurs under the following conditions:

- correction pulse after a missing step (both modes)
- end-of-life mode
- if stage 5 is not enough to turn the motor (both modes)



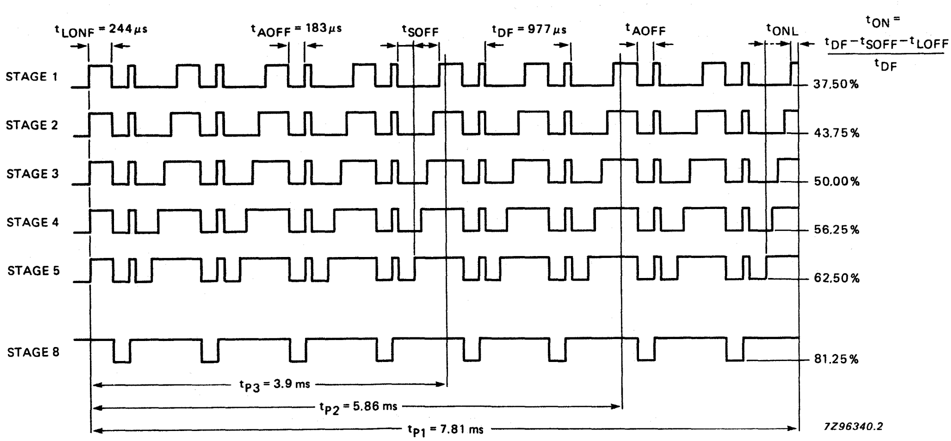
t_{OFF} for stage 1 to 5 = 488 µs − stage x 61 µs

t_{ON} for stage 1 to 5 = 488 µs + stage x 61 µs

Fig.4 Motor pulses in the silver-oxide mode (V_{DD} = 1.55 V).

DEVELOPMENT DATA

In the silver-oxide mode, the ON state of the motor pulse varies between 56.25% and 100% of the duty factor t_{DF} = 977 µs depending on the stage (Fig.4). It increases in steps of 6.25% per stage. In the lithium mode, the ON state of the motor pulse is reduced by 18.75% of the duty factor t_{DF} (Fig.5) to compensate for the increase in the voltage level.



t_{OFF} for stage 1 to 5 = 672 µs − stage x 61 µs

t_{ON} for stage 1 to 5 = 305 µs + stage x 61 µs

Fig.5 Motor pulses in the lithium mode (V_{DD} = 2.1 V).

Motor pulses (continued)

After a RESET the circuit always starts with stage 1. The circuit continues to operate in stage 1, when all motor pulses have been executed. A failure to execute all motor pulses results in the circuit going into stage 2, this sequence will be repeated through to stage 8.

When the motor pulses at stage 5 are not large enough to turn the motor, stage 8 is implemented for a maximum of 8 minutes with no attempt to keep current consumption low. After stage 8 has been executed the procedure is repeated from RESET.

The circuit operates for 8 minutes at a fixed stage, if every motor pulse is executed. The next 480 motor pulses are then produced at the next lower stage unless a missing step is detected. If a step is missed a correction sequence is produced and for a maximum of 8 minutes the motor pulses are increased by one stage.

Voltage level detector

The supply voltage is compared with the internal voltage reference V_{LIT} and V_{EOL} every minute. The first voltage level detection is carried out 30 ms after RESET.

When a lithium voltage level is detected ($V_{DD} \geq V_{LIT}$), the circuit starts operating in the lithium mode (Fig.5).

When the detected V_{DD} voltage level is between V_{LIT} and V_{EOL}, the circuit operates in the silver-oxide mode (Fig.4).

If the battery end-of-life isdetected ($V_{DD} < V_{EOL}$), the detection and stage control is switched OFF and the waveform produced is an unchopped version of the stage 8 waveform. To indicate this condition the waveform is produced in bursts of 4 pulses every 4 s.

Detection of motor movement

After a motor pulse, the motor is shorted to V_{DD} for 1 ms. Afterwards the energy in the motor inductor will be dissipated to measure only the current generated by the induced motor voltage. During the time t_{DI} (dissipation of energy time) all switches shown in Fig.6 are open to reduce the current as fast as possible. The current will now flow through the diodes D3 and D2, or D4 and D1. Then the first of 52 possible measurement cycles (t_{MC}) starts to measure the induced current.

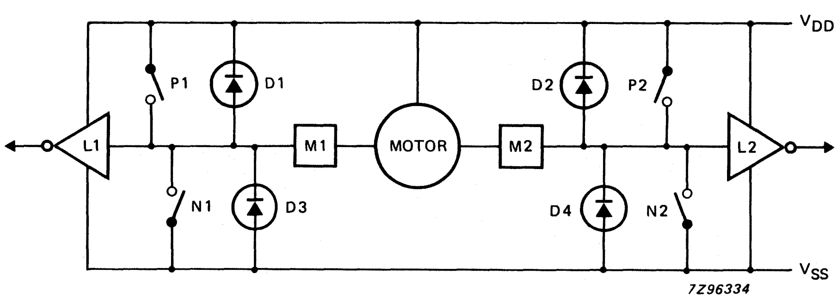


Fig.6 Motor driving and detecting circuit.

Detection criterion (Figs 7 and 8)

Part 1

- P = 2 number of measured positive current polarities after t_{DI}.

Part 2

- N = 3 number of measured positive current polarities since the first negative current polarity is detected after part 1 (see Fig.7).

If the opposite polarity is measured in one part, the internal counter is reset, so the results of all measurements in this part are ignored.

The waveform of the induced current must enable all these measurements within the time t_D after the end of a positive motor pulse in order to be accepted as a waveform of an executed motor pulse.

If the detection criterion is satisfied earlier, a measurement cycle will not be started and the switches P1 and P2 stay closed, the motor is switched to V_{DD}.

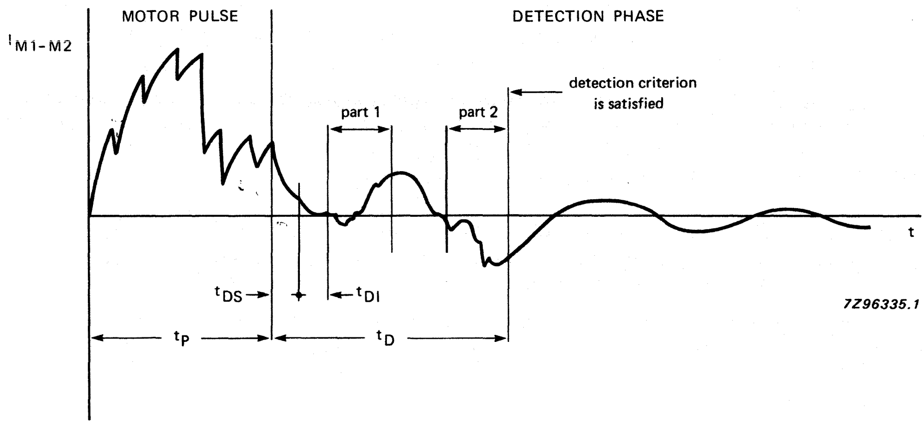


Fig.7 Typical current waveform of a successfully executed motor pulse.

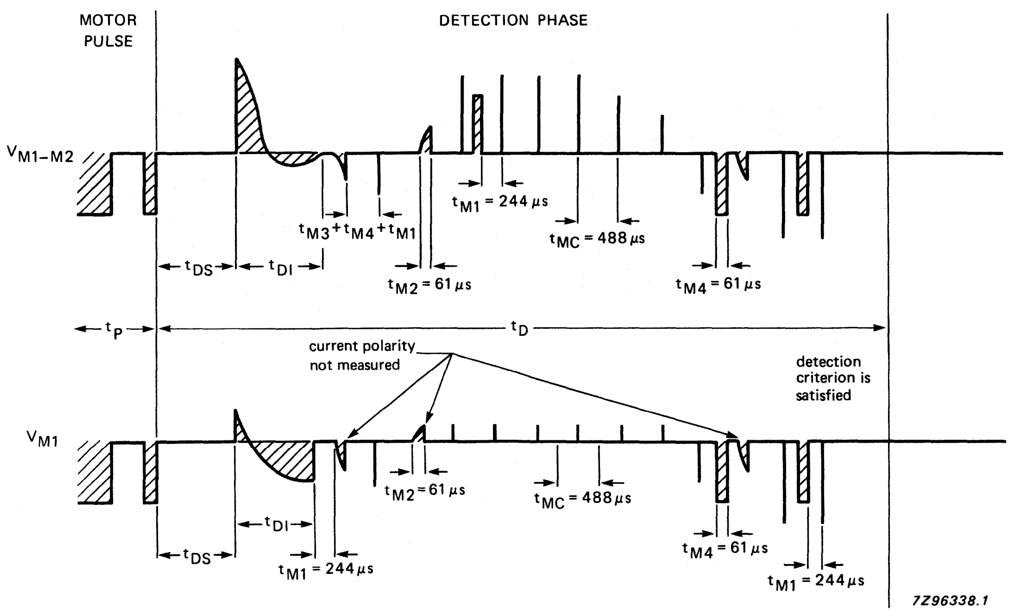


Fig.8 Detection phase of the current waveform in Fig.7.

Detection criterion (continued)

Every measurement cycle (t_{MC}) has 4 phases, they are as follows:

Phase 1: (t_{M1}) During t_{M1} the switches P1 and P2 are closed in order to switch the motor to V_{DD}, so the induced current flows unaffected through the motor inductance.

Phase 2: (t_{M2}) Measures the induced current. During a maximum time t_{M2} all switches are open until a change is sensed by one of the level detectors (L1, L2). The motor is shorted to V_{DD}. Depending on the direction of the interrupted current:

- the current flows through diodes D3 and D2, causing the voltage at M1 to decrease in relation to M2;
- the current flows through diodes D4 and D1, causing the voltage at M2 to decrease in relation to M1.

A successfully detected current polarity is normally characterized by a short pulse of 0.5 to 10 μs with a voltage up to ± 2.6 V, failed polarity detection by the maximum pulse width of 61 μs and a voltage of ± 0.5 V (see Fig.8).

Phase 3: (t_{M3}) The switches P1 and P2 remain closed for the time t_{M3}.

Phase 4: (t_{M4}) If the circuit detects less pulses than P and N respectively, a pulse of the time t_{M4} occurs to reduce the induced current. Therefore P2 and P1 are opened and N1 and N2 are closed. Otherwise P1 and P2 remain closed.

Detection and pulse width control will be switched OFF, when the battery voltage is below the end-of-life voltage (V_{EOL}) or if stage 5 is not sufficient to turn the motor.

Correction sequence

If a missing step is detected, a correction sequence is produced. This consists of a small pulse (t_{C1}) which gives the motor a defined position and after 29.30 ms a pulse of stage 8 (t_{C2}) to turn the motor.

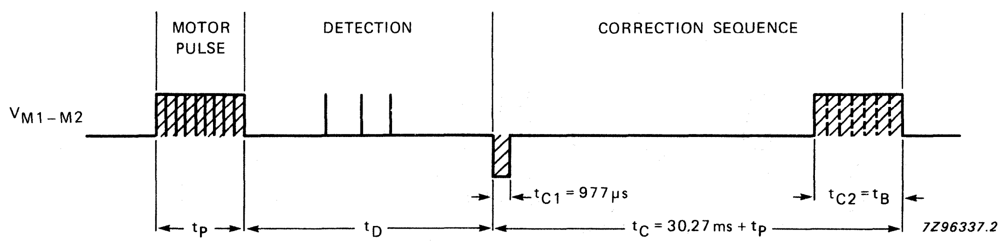


Fig.9 Correction sequence after a missing motor step with motor connected.

Timekeeping adjustment *

To compensate for the tolerance in the quartz crystal frequency, a number (n) of 8192 Hz are inhibited every minute of operation. The number (n) is stored in a non-volatile memory, which is achieved by the following steps (see Fig.11):

1. The quartz frequency deviation (Δf/f) and n are found (see Table 1).
2. V_{DD} is increased to 5.1 V allowing the contents of the EEPROM to be checked from the motor pulse period t_{T3}.
3. V_{DD} is decreased to 2.5 V during a motor pulse to initialize a storing sequence.
4. The first V_{DD} pulse to 5 V erases the contents of EEPROM.
5. When the EEPROM is erased a logic 1 is at the TEST pin.
6. V_{DD} is increased to 5.1 V to read the data by pulsing V_{DD} n times to 4.5 V. After the n edge, V_{DD} is decreased to 2.5 V.
7. V_{DD} is increased to 5.1 V to write the EEPROM and reset the circuit.
8. V_{DD} is decreased to the operating voltage level to terminate the storing sequence and to return to operating mode.
9. V_{DD} is increased to 5.1 V to check writing from the motor pulse period t_{T3}.
10. V_{DD} is decreased to the operation voltage between two motor pulses to return to operating mode.

Table 1 Quartz crystal frequency deviation and n

$\frac{\Delta f}{f} \times 10^{-6}$	n	t_{T3} (ms) step 2 or 9
+ 2.03	1	31.372
+ 4.06	2	31.494
.	.	.
.	.	.
.	.	.
+ 127.89	63	38.936

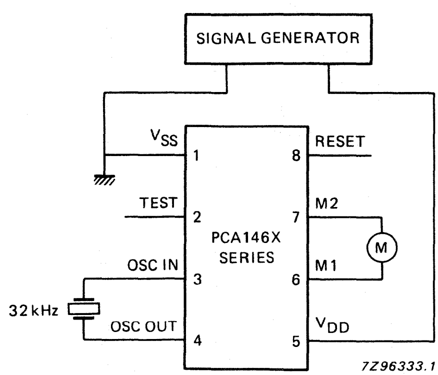
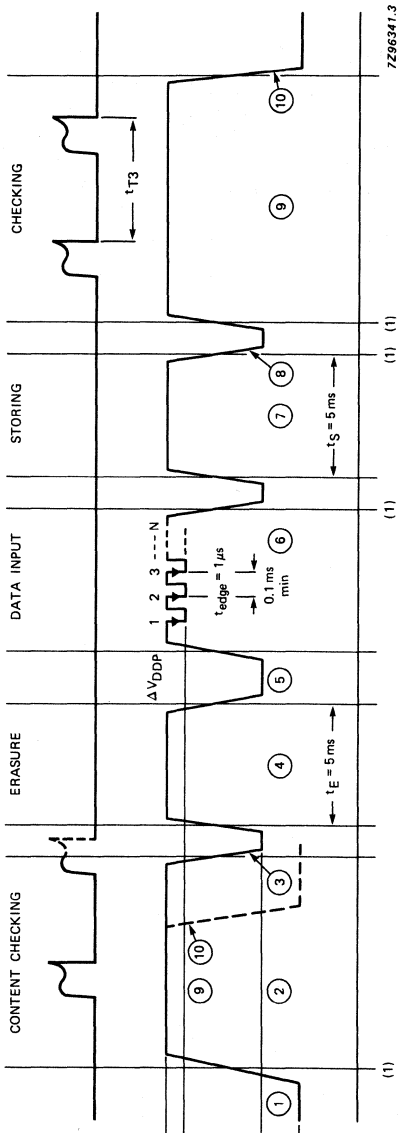


Fig.10 Programming circuit diagram.

* Programming can be performed ten times.



(1) Rise and fall time should be larger than 1 ms for immediately correct checking.

Fig.11 V_{DD} for programming.

Power-on reset

For correct operation of the power-on reset the rise time of V_{DD} from 0 V to 2.1 V should be less than 0.1 ms. All resetable flip-flops ara reset. Additionally the polarity of the first motor pulse is positive: $V_{M1} - V_{M2} \geqslant 0$ V.

Customer testing

An output frequency of 32 Hz is provided at RESET (pin 8) to be used for exact frequency measurement. Every minute a jitter occurs as a result of the inhibition, which occurs 90 to 150 ms after disconnecting the RESET from V_{DD}.

Connecting the RESET to V_{DD} stops the motor pulses leaving them in a 3-state mode and sets the motor pulse width for the next available motor pulse to stage 1 in the silver-oxide mode. A 32 Hz signal without-jitter is produced at the TEST pin. Debounce time RESET = 13.7 to 78.1 ms.

Connecting RESET to V_{SS} activates tests 1 and 2 and disables the inhibition.

In test 1 ($V_{DD} > V_{EOL}$) normal function takes place except the motor pulse period is t_{T1} = 125 ms instead of t_T and the motor pulse stage is reduced every second instead of every 8 minutes. At TEST a speeded-up 8 minute signal is available.

Test 2: if V_{DD} becomes lower than V_{EOL} motor pulses of stage 8 with a time period of t_{T2} = 31.25 ms are produced.

Test and reset mode are terminated by disconnecting the RESET pin.
Test 3: when V_{DD} voltage level is greater than 5.1 V, motor pulses of stage 8 with a time period of t_{T3} = 31.25 ms and n x 122 μs are produced to check the contents of the EEPROM. At TEST a speeded-up cycle for motor pulse period signal t_T is available at 1024 times its normal frequency. Decreasing V_{DD} voltage level to lower than 2.5 V between two motor pulses returns the circuit to normal operating conditions.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (V_{SS} = 0 V); note 1	V_{DD}	−1.8 to + 5 V
All input voltages; note 2	V_I	V_{SS} to V_{DD} V
Output short-circuit duration		indefinite
Operating ambient temperature range	T_{amb}	−10 to + 60 °C
Storage temperature range	T_{stg}	−30 to + 100 °C

Notes to the Ratings

1. Connecting the battery with reversed polarity does not destroy the circuit, but in this condition a large current flows, which will rapidly discharge the battery.
2. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisible to take handling precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 1.55 V; V_{SS} = 0 V; f_{osc} = 32.768 kHz; T_{amb} = 25 °C; crystal: R_S = 20 kΩ; C_1 = 2 to 3 fF; C_L = 8 to 10 pF; C_o = 1 to 3 pF; unless otherwise specified.
Immunity against parasitic impedance = 20 MΩ from one pin to an adjacent pin.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	T_{amb} = −10 to +60 °C	V_{DD1}	1.2	1.55	2.5	V
Supply voltage	transient within 1.2 V and 2.5 V	ΔV_{DD}	–	–	0.25	V
Supply voltage	programming	V_{DD2}	5.0	5.1	5.2	V
Supply voltage pulse	programming	ΔV_{DDP}	0.55	0.6	0.65	V
Supply current	between motor pulses	I_{DD1}	–	170	260	nA
Supply current	V_{DD} = 2.10 V	I_{DD2}	–	190	300	nA
Supply current	stop mode; pin 8 connected to V_{DD}	I_{DD3}	–	180	280	nA
Supply current	V_{DD} = 2.10 V	I_{DD4}	–	220	360	nA
Supply current	T_{amb} = −10 to +60 °C	I_{DD5}	–	–	600	nA
Motor output						
Saturation voltage Σ (P + N)	R_M = 2 kΩ; T_{amb} = −10 to +60 °C	V_{sat}	–	150	200	mV
Output short-circuit impedance	between motor pulses $I_{transistor}$ < 1 mA	R_{os}	–	200	300	Ω
Oscillator						
Starting voltage		$V_{OSC\ ST}$	1.2	–	–	V
Transconductance	$V_{i(p-p)} \leq 50$ mV	g_m	6	15	–	μS
Start-up time		t_{osc}	–	1	–	s
Frequency stability	ΔV_{DD} = 100 mV	$\Delta f/f$	–	0.05×10^{-6}	0.3×10^{-6}	
Frequency tolerance	device-to-device	$\Delta f/f$	–	$\pm 3 \times 10^{-6}$	$\pm 10 \times 10^{-6}$	
Input capacitance		C_i	8	10	12	pF
Output capacitance		C_o	12	15	18	pF
Voltage level detector						
Threshold voltage		V_{LIT} V_{EOL}	1.65 1.27	1.80 1.35	1.95 1.46	V V
Hysteresis of threshold		ΔV_{EOL}	–	10	–	mV
Temperature coefficient		$\frac{\Delta V_{EOL}}{dT}$	–	−1	–	mV/K

parameter	conditions	symbol	min.	typ.	max.	unit
Reset input						
Output frequency		f_o	–	32	–	Hz
Output voltage swing	R = 1 MΩ; C = 10 pF	ΔV_o	1.4	–	–	V
Edge time	R = 1 MΩ; C = 10 pF	t_{edge}	–	1	–	s
Peak input current	note 1	I_{im}	–	320	–	nA
Average input current		$I_{i(av)}$	–	10	–	nA

Note

1. Duty factor is 1:32 and RESET = V_{DD} or V_{SS}.

Table 1 Available types

type	pulse width t_P (ms)	period t_T (s)	EOL	lithium	detection criterion	EEPROM
PCA1460	7.8	1	yes	yes	P = 3; N = 5	yes
PCA1461	7.8	1	no	yes	P = 2; N = 3	yes
PCA1462	5.8	1	yes	yes	P = 2; N = 3	yes
PCA1463	3.9	1	yes	yes	P = 2; N = 3	yes
PCA1464	3.9	1	no	no	P = 2; N = 3	yes
PCA1465	5.8	1	no	no	P = 1; N = 2	yes
PCA1466	5.8	5	no	yes	P = 1; N = 2	no
PCA1467	7.8	1	no	yes	P = 2; N = 3	yes
PCA1468	7.8	1	yes	no	P = 3; N = 5	no

DEVELOPMENT DATA

TIMING PARAMETERS

section	remark	symbol	value	option	unit
Motor pulse Figs 3, 4 and 5	cycle for motor pulse*	t_T	1	5, 10, 12 or 20	s
	motor pulse width	t_P	7.81	3.9 or 5.9	ms
	duty factor	t_{DF}	977		µs
	last duty factor on	t_{ONL}	61 to 305		µs
Level mode	voltage detection cycle	t_v	60		s
Silver-oxide mode Fig.4	duty factor on	t_{SON}	550 to 794		µs
	duty factor off	t_{SOFF}	427 to 183		µs
	first duty factor on	t_{SONF}	488		µs
Lithium mode Fig.5	additional duty factor off	t_{AOFF}	183		µs
	duty factor on	t_{LON}	305 to 611		µs
	duty factor off	t_{LOFF}	672 to 366		µs
	first duty factor on	t_{LONF}	244		µs
End-of-life mode Fig.11	EOL sequence	t_E	4		s
	motor pulse width	t_{E1}	t_P		ms
	time between pulses	t_{E2}	31.25		ms
Detection Fig.8	detection sequence	t_D	4.3 to 28.3		ms
	short-circuited motor	t_{DS}	997		µs
	dissipation of energy	t_{DI}	977		µs
	measurement cycle	t_{MC}	488		µs
	phase 1	t_{M1}	244		µs
	phase 2 (measure window)	t_{M2}	61		µs
	phase 3	t_{M3}	122		µs
	phase 4	t_{M4}	61		µs
	positive current polarities	P	2	1 to 6	
	negative current polarities	N	3	1 to 6	
Correction sequence Fig.9	correction sequence	t_C	t_P + 30.27		ms
	small pulse width	t_{C1}	977		µs
	large pulse width	t_{C2}	t_P		ms
Testing	cycles for motor				
	pulses in: Test 1	t_{T1}	125		ms
	Test 2	t_{T2}	31.25		ms
Fig.11	Test 3	t_{T3}	31.25 or 39		ms
	debounce time for RESET = V_{DD}	t_{DEB}	13.7 to 78.1		ms

* No option available when EOL indication is required.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS

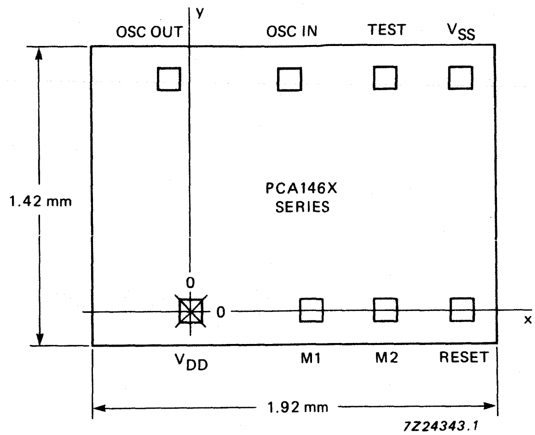


Fig.12 Bonding pad locations.

Bonding pad dimensions 110 μm x 110 μm
Chip area = 2.73 mm^2

Table 1 Bonding pad locations (dimensions in μm)

All x, y co-ordinates are referenced to the bottom left pad (V_{DD}), see Fig.12.

pad	x	y
V_{SS}	1290	1100
TEST	940	1100
OSC IN	481	1100
OSC OUT	−102	1100
V_{DD}	0	0
M1	578	0
M2	930	0
STOP	1290	0
chip corner max. value	−470	−160

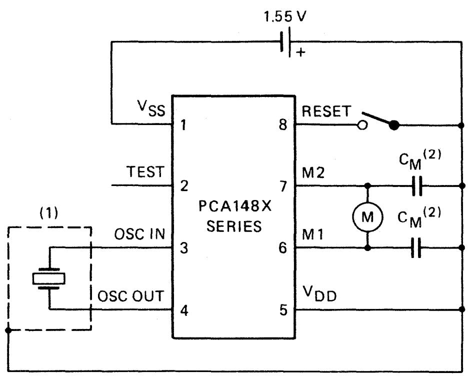
32 kHz WATCH CIRCUIT WITH ADAPTIVE MOTOR PULSE

GENERAL DESCRIPTION

The PCA148X series are CMOS integrated circuits specially suited for battery-operated, quartz-crystal-controlled wrist-watches, with a bipolar stepping motor.

Features

- 32 kHz oscillator, amplitude regulated with excellent frequency stability
- High immunity of the oscillator to leakage currents
- Timekeeping adjustment electrically programmable and reprogrammable (via EEPROM)
- A quartz crystal is the only external component required
- Very low current consumption: typically 170 nA
- Output for bipolar stepping motors of different types
- Up to 50% reduction in motor current, compared with conventional circuits, by self adaption of the motor pulse width according to the required torque of the motor
- No loss of motor steps possible because of on-chip detection of the induced motor voltage
- Indication for battery end-of-life
- Stop function for accurate timing
- Power-on reset for fast testing
- Various test modes for testing the mechanical parts of the watch as well as the IC itself



(1) Quartz crystal case should be connected to V_{DD}. Stray capacitance and leakage resistance from RESET, M1 or M2 to OSC IN should be less than 0.5 pF or larger than 20 MΩ.

(2) Motor, probe and stray capacitance from M2 or M1 to V_{DD} or V_{SS} should be less than C_M = 80 pF for correct operation of the detection circuit. Driving the motor at its minimum energy, probe and stray capacitance must be avoided.

Fig.1 Typical application circuit diagram.

PACKAGE OUTLINES

PCA148XT: 8-lead micro-flat-pack; plastic (SOT144).
PCA148XU: chip in tray.

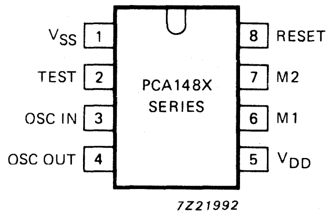


Fig.2 Pinning diagram.

PINNING

1	V_{SS}	ground (0 V)
2	TEST	test input
3	OSC IN	oscillator input
4	OSC OUT	oscillator output
5	V_{DD}	supply voltage
6	M1	motor 1 output
7	M2	motor 2 output
8	RESET	reset input

FUNCTIONAL DESCRIPTION AND TESTING

The motor output delivers pulses of six different stages depending on the torque required to turn the motor (Fig.4). Every motor pulse is followed by a detection phase which monitors the waveform of the induced motor voltage. When a step is missed a correction sequence will be started (Fig.3).

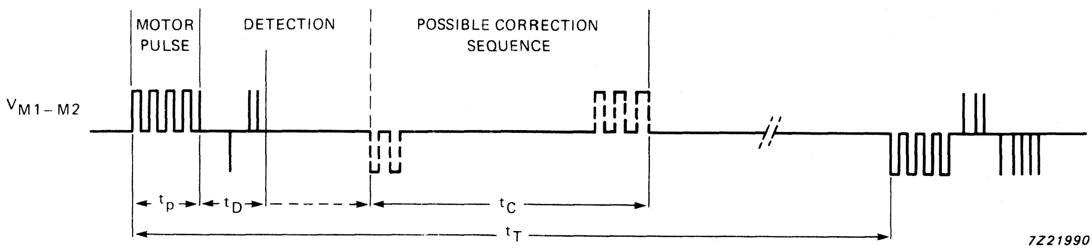


Fig.3 Possible motor output waveform in normal operation with motor connected.

Motor pulses

The circuit produces motor pulses of six different stages (stage 1 to 5, stage 6).

Stages 1 to 5 are used in normal operation, stage 6 occurs under the following conditions:

- correction pulse after a missing step
- end-of-life mode
- if stage 5 is not enough to turn the motor

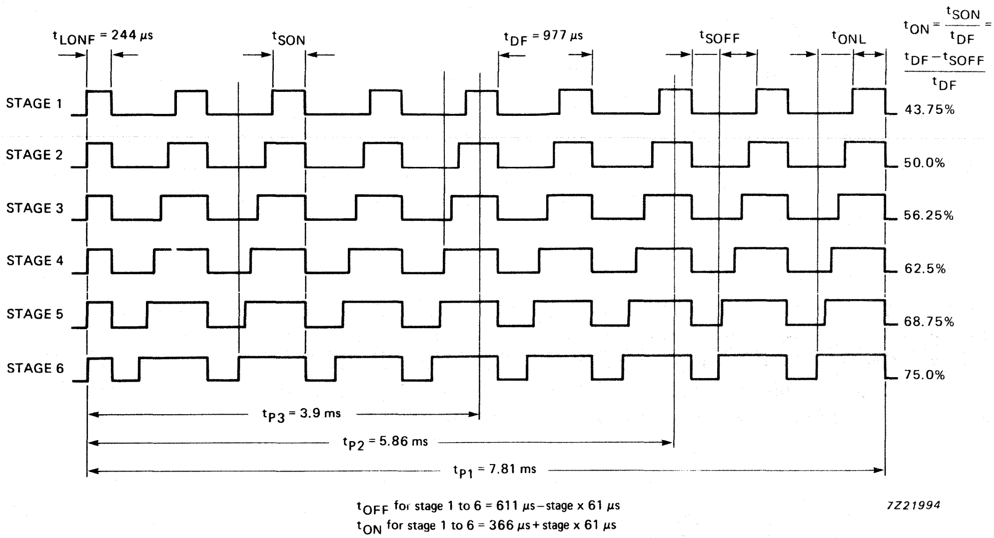


Fig.4 Motor pulses (V_{DD} = 1.55 V).

In the silver-oxide mode, the ON state of the motor pulse varies between 56.25% and 100% of the duty factor t_{DF} = 977 μs depending on the stage (Fig.4). It increases in steps of 6.25% per stage.

In the lithium mode, the ON state of the motor pulse is reduced by 18.75% of the duty factor t_{DF} (Fig.5) to compensate for the increase in the voltage level.
After a RESET the circuit always starts with stage 1. The circuit continues to operate in stage 1, when all motor pulses have been executed. A failure to execute all motor pulses results in the circuit going into stage 2, this sequence will be repeated through to stage 6.

When the motor pulses at stage 5 are not large enough to turn the motor, stage 6 is implemented for a maximum of 8 minutes with no attempt to keep current consumption low. After stage 6 has been executed the procedure is repeated from RESET.

The circuit operates for 8 minutes at a fixed stage, if every motor pulse is executed. The next 480 motor pulses are then produced at the next lower stage unless a missing step is detected. If a step is missed a correction sequence is produced and for a maximum of 8 minutes the motor pulses are increased by one stage.

Voltage level detector

The supply voltage is compared with the internal voltage reference V_{EOL} every minute. The first voltage level detection is carried out 30 ms after RESET.

When the detected V_{DD} voltage level is greater than V_{EOL}, the circuit operates in normal mode (Fig.4).

If the battery end-of-life is detected ($V_{DD} < V_{EOL}$), the detection and stage control is switched OFF and the waveform of stage 6 will be executed. To indicate this condition the waveform is produced in bursts of 4 pulses every 4 s.

Detection of motor movement

After a motor pulse, the motor is shorted to V_{DD} for 1 ms. Afterwards the energy in the motor inductor will be dissipated to measure only the current generated by the induced motor voltage. During the time t_{DI} (dissipation of energy time) all switches shown in Fig.5 are open to reduce the current as fast as possible. The current will now flow through the diodes D3 and D2, or D4 and D1. Then the first of 52 possible measurement cycles (t_{MC}) starts to measure the induced current.

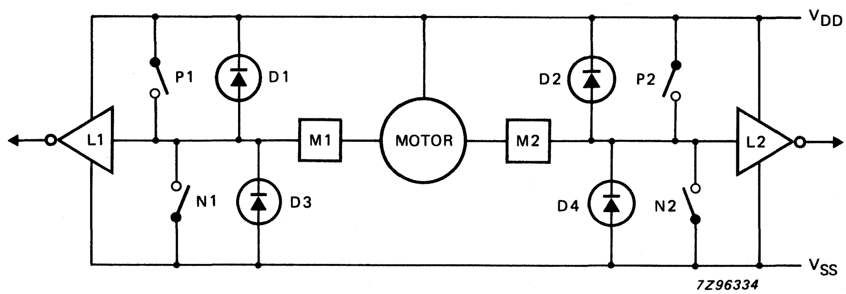


Fig.5 Motor driving and detecting circuit.

Detection criterion (Figs 6 and 7)

Part 1

- P = 2 number of measured positive current polarities after t_{DI}.

Part 2

- N = 3 number of measured positive current polarities since the first negative current polarity is detected after part 1 (see Fig.6).

If the opposite polarity is measured in one part, the internal counter is reset, so the results of all measurements in this part are ignored.

The waveform of the induced current must enable all these measurements within the time t_D after the end of a positive motor pulse in order to be accepted as a waveform of an executed motor pulse.

If the detection criterion is satisfied earlier, a measurement cycle will not be started and the switches P1 and P2 stay closed, the motor is switched to V_{DD}.

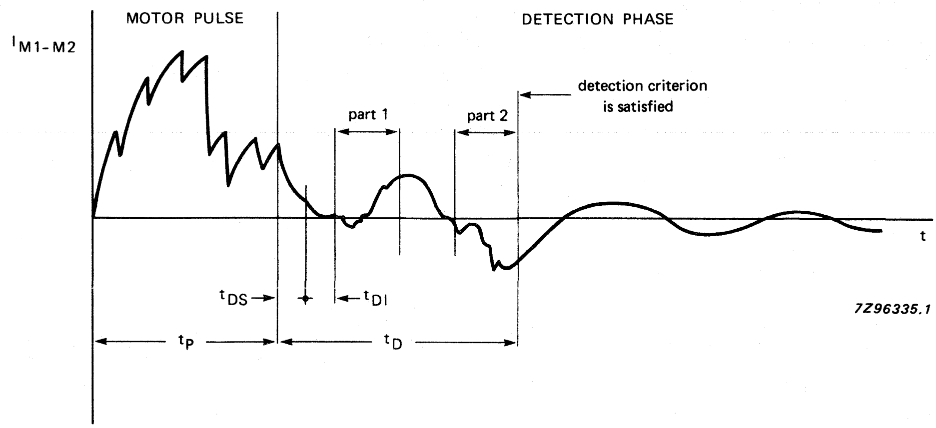


Fig.6 Typical current waveform of a successfully executed motor pulse.

DEVELOPMENT DATA

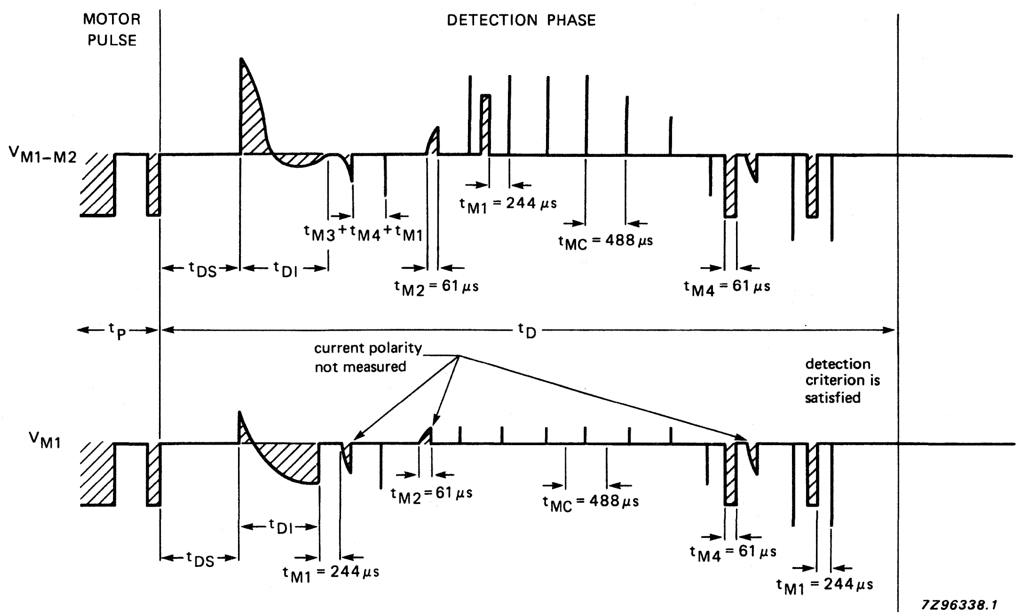


Fig.7 Detection phase of the current waveform in Fig.7.

Detection criterion (continued)

Every measurement cycle (t_{MC}) has 4 phases, they are as follows:

Phase 1: (t_{M1}) During t_{M1} the switches P1 and P2 are closed in order to switch the motor to V_{DD}, so the induced current flows unaffected through the motor inductance.

Phase 2: (t_{M2}) Measures the induced current. During a maximum time t_{M2} all switches are open until a change is sensed by one of the level detectors (L1, L2). The motor is shorted to V_{DD}. Depending on the direction of the interrupted current:

- the current flows through diodes D3 and D2, causing the voltage at M1 to decrease in relation to M2;
- the current flows through diodes D4 and D1, causing the voltage at M2 to decrease in relation to M1.

A successfully detected current polarity is normally characterized by a short pulse of 0.5 to 10 μs with a voltage up to ± 2.6 V, failed polarity detection by the maximum pulse width of 61 μs and a voltage of ± 0.5 V (see Fig.7).

Phase 3: (t_{M3}) The switches P1 and P2 remain closed for the time t_{M3}.

Phase 4: (t_{M4}) If the circuit detects less pulses than P and N respectively, a pulse of the time t_{M4} occurs to reduce the induced current. Therefore P2 and P1 are opened and N1 and N2 are closed. Otherwise P1 and P2 remain closed.

Detection and pulse width control will be switched OFF, when the battery voltage is below the end-of-life voltage (V_{EOL}) or if stage 5 is not sufficient to turn the motor.

Correction sequence

If a missing step is detected, a correction sequence is produced. This consists of a small pulse (t_{C1}) which gives the motor a defined position and after 29.30 ms a pulse of stage 6 (t_{C2}) to turn the motor.

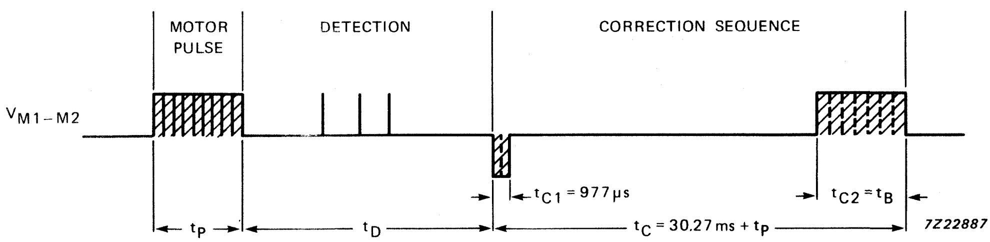


Fig.8 Correction sequence after a missing motor step with motor connected.

Timekeeping adjustment *

To compensate for the tolerance in the quartz crystal frequency, a number (n) of 8192 Hz are inhibited every minute of operation. The number (n) is stored in a non-volatile memory, which is achieved by the following steps (see Fig.10):

1. The quartz frequency deviation ($\Delta f/f$) and n are found (see Table 1).
2. V_{DD} is increased to 5.1 V allowing the contents of the EEPROM to be checked from the motor pulse period t_{T3}.
3. V_{DD} is decreased to 2.5 V during a motor pulse to initialize a storing sequence.
4. The first V_{DD} pulse to 5.1 V erases the contents of EEPROM.
5. When the EEPROM is erased a logic 1 is at the TEST pin.
6. V_{DD} is increased to 5.1 V to read the data by pulsing V_{DD} n times to 4.5 V. After the n edge, V_{DD} is decreased to 2.5 V.
7. V_{DD} is increased to 5.1 V to write the EEPROM and reset the circuit.
8. V_{DD} is decreased to the operating voltage level to terminate the storing sequence and to return to operating mode.
9. V_{DD} is increased to 5.1 V to check writing from the motor pulse period t_{T3}.
10. V_{DD} is decreased to the operation voltage between two motor pulses to return to operating mode.

Table 1 Quartz crystal frequency deviation and n

$\frac{\Delta f}{f} \times 10^{-6}$	n	t_{T3} (ms) step 2 or 9
+ 2.03	1	31.372
+ 4.06	2	31.494
.	.	.
.	.	.
.	.	.
+ 127.89	63	38.936

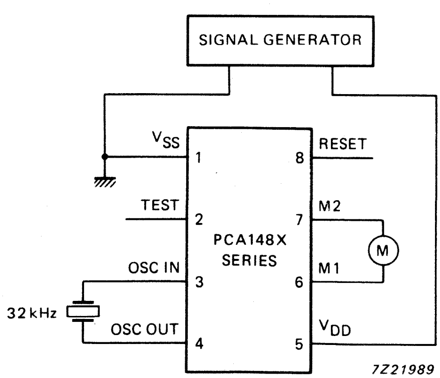
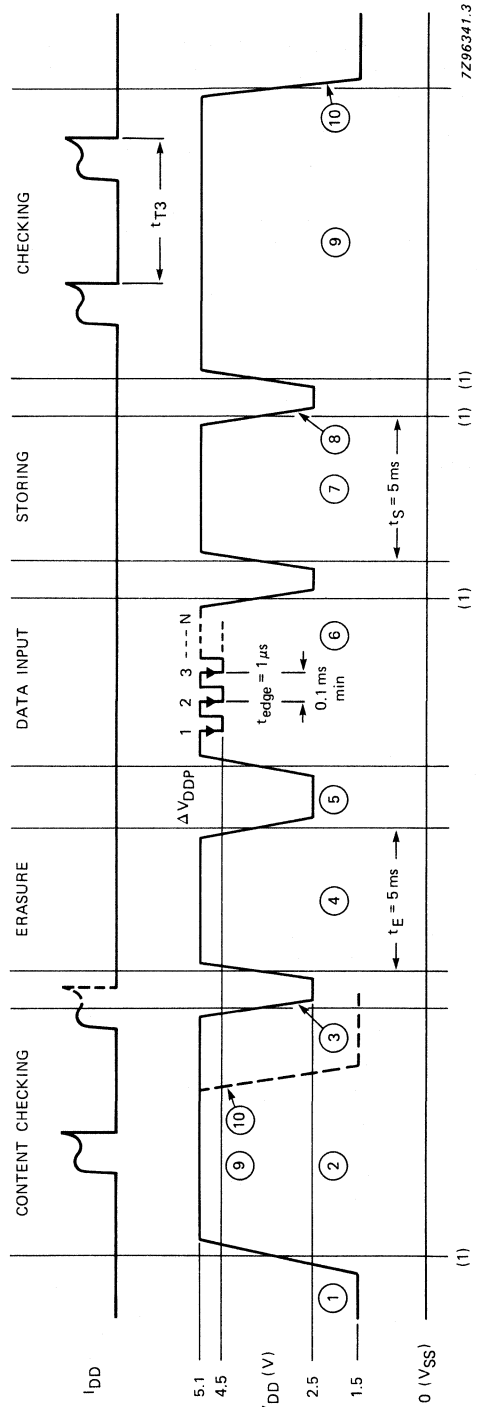


Fig.9 Programming circuit diagram.

* Programming can be performed ten times.



(1) Rise and fall time should be larger than 1 ms for immediately correct checking.

Fig.10 V_{DD} for programming.

Power-on reset

For correct operation of the power-on reset the rise time of V_{DD} from 0 V to 2.1 V should be less than 0.1 ms. All resetable flip-flops are reset. Additionally the polarity of the first motor pulse is positive: $V_{M1} - V_{M2} \geqslant 0$ V.

Customer testing

An output frequency of 32 Hz is provided at RESET (pin 8) to be used for exact frequency measurement. Every minute a jitter occurs as a result of the inhibition, which occurs 90 to 150 ms after disconnecting the RESET from V_{DD}.

Connecting the RESET to V_{DD} stops the motor pulses leaving them in a 3-state mode and sets the motor pulse width for the next available motor pulse to stage 1. A 32 Hz signal without jitter is produced at the TEST pin. Debounce time RESET = 13.7 to 78.1 ms.

Connecting RESET to V_{SS} activates tests 1 and 2 and disables the inhibition.

In test 1 ($V_{DD} > V_{EOL}$) normal function takes place except the motor pulse period is t_{T1} = 125 ms instead of t_T and the motor pulse level is reduced every second instead of every 8 minutes. At TEST a speeded-up 8 minute signal is available.

TEST 2: if V_{DD} becomes lower than V_{EOL} motor pulses of stage 6 with a time period of t_{T2} = 31.25 ms are produced.

Test and reset mode are terminated by disconnecting the RESET pin.

TEST 3: when V_{DD} voltage level is greater than 5.1 V, motor pulses without chopping and a time period of t_{T3} = 31.25 ms and n x 122 µs are produced to check the contents of the EEPROM. At TEST a speeded-up cycle for motor pulse period signal t_T is available at 1024 times its normal frequency. Decreasing V_{DD} voltage level to lower than 2.5 V between two motor pulses returns the circuit to normal operating conditions.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (V_{SS} = 0 V); note 1	V_{DD}	−1.8 to + 6 V
All input voltages; note 2	V_I	V_{SS} to V_{DD} V
Output short-circuit duration		indefinite
Operating ambient temperature range	T_{amb}	−10 to + 60 °C
Storage temperature range	T_{stg}	−30 to + 100 °C

Notes to the Ratings

1. Connecting the battery with reversed polarity does not destroy the circuit, but in this condition a large current flows, which will rapidly discharge the battery.
2. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisible to take handling precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 1.55 V; V_{SS} = 0 V; f_{osc} = 32.768 kHz; T_{amb} = 25 °C; crystal: R_S = 20 kΩ; C_1 = 2 to 3 fF; C_L = 8 to 10 pF; C_o = 1 to 3 pF; unless otherwise specified.
Immunity against parasitic impedance = 20 MΩ from one pin to an adjacent pin.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	T_{amb} = −10 to +60 °C	V_{DD1}	1.2	1.55	2.5	V
Supply voltage	transient	ΔV_{DD}	–	–	0.25	V
Supply voltage	programming	V_{DD2}	5.0	5.1	5.2	V
Supply voltage pulse	programming	ΔV_{DDP}	0.55	0.60	0.65	V
Supply current	between motor pulses	I_{DD1}	–	170	260	nA
Supply current	stop mode; pin 8 connected to V_{DD}	I_{DD3}	–	180	280	nA
Motor output						
Saturation voltage Σ (P + N)	R_M = 2 kΩ; T_{amb} = −10 to +60 °C	V_{sat}	–	150	200	mV
Output short-circuit impedance	between motor pulses $I_{transistor}$ < 1 mA	R_{os}	–	200	300	Ω
Oscillator						
Starting voltage		$V_{OSC\ ST}$	1.2	–	–	V
Transconductance	$V_{i(p-p)} \leq 50$ mV	g_m	6	15	–	µS
Start-up time		t_{osc}	–	1	–	s
Frequency stability	ΔV_{DD} = 100 mV	Δf/f	–	0.05×10^{-6}	0.3×10^{-6}	
Frequency tolerance	device-to-device	Δf/f	–	$\pm 3 \times 10^{-6}$	$\pm 10 \times 10^{-6}$	
Input capacitance		C_i	8	10	12	pF
Output capacitance		C_o	12	15	18	pF
Voltage level detector						
Threshold voltage		V_{EOL}	1.30	1.38	1.46	V
Hysteresis of threshold		ΔV_{EOL}	–	10	–	mV
Temperature coefficient		$\frac{\Delta V_{EOL}}{dT}$	–	−1	–	mV/K

parameter	conditions	symbol	min.	typ.	max.	unit
Reset input						
Output frequency		f_o	–	32	–	Hz
Output voltage swing	R = 1 MΩ; C = 10 pF	ΔV_o	1.4	–	–	V
Edge time	R = 1 MΩ; C = 10 pF	t_{edge}	–	1	–	s
Peak input current	note 1	I_{im}	–	320	–	nA
Average input current		$I_{i(av)}$	–	10	–	nA

Note

1. Duty factor is 1:32 and RESET = V_{DD} or V_{SS}.

Table 1 Available tyoes

type	pulse width t_P (ms)	period t_T (s)	EOL	detection criterion	EEPROM
PCA1481	7.81	1	yes	P = 3; N = 5	yes
PCA1482	5.86	1	yes	P = 2; N = 3	yes

DEVELOPMENT DATA

TIMING PARAMETERS

section	remark	symbol	value	option	unit
Motor pulse Figs 3 and 4	cycle for motor pulse*	t_T	1	5, 10, 12 or 20	s
	motor pulse width	t_P	7.81	3.9 or 5.9	ms
	duty factor	t_{DF}	977		μs
	last duty factor on	t_{ONL}	183 to 488		μs
Level mode	voltage detection cycle	t_V	60		s
Silver-oxide mode Fig.4	duty factor on	t_{SON}	427 to 733		μs
	duty factor off	t_{SOFF}	550 to 244		μs
	first duty factor on	t_{SONF}	244		μs
End-of-life mode Fig.10	EOL sequence	t_E	4		s
	motor pulse width	t_{E1}	t_P		ms
	time between pulses	t_{E2}	31.25		ms
Detection Fig.7	detection sequence	t_D	4.3 to 28.3		ms
	short-circuited motor	t_{DS}	977		μs
	dissipation of energy	t_{DI}	977		μs
	measurement cycle	t_{MC}	488		μs
	phase 1	t_{M1}	244		μs
	phase 2 (measure window)	t_{M2}	61		μs
	phase 3	t_{M3}	122		μs
	phase 4	t_{M4}	61		μs
	positive current polarities	P	2	$P < N$	
	negative current polarities	N	3	2 to 6	
Correction sequence Fig.8	correction sequence	t_C	$t_P + 30.27$		ms
	small pulse width	t_{C1}	977		μs
	large pulse width	t_{C2}	t_P		ms
Testing	cycles for motor				
	pulses in: Test 1	t_{T1}	125		ms
	Test 2	t_{T2}	31.25		ms
Fig.10	Test 3	t_{T3}	31.25 or 39		ms
	debounce time for RESET = V_{DD}	t_{DEB}	13.7 to 78.1		ms

* No option available when EOL indication is required.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS

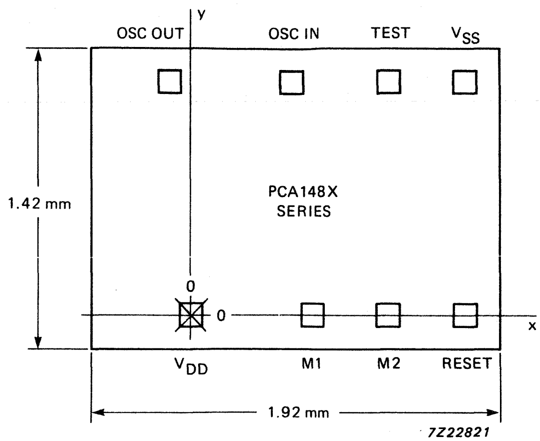


Fig.11 Bonding pad locations.

Bonding pad dimensions 110 μm x 110 μm
Chip area = 2.73 mm^2

Table 1 Bonding pad locations (dimensions in μm)

All x, y co-ordinates are referenced to the bottom left pad (V_{DD}), see Fig. 11.

pad	x	y
V_{SS}	1290	1100
TEST	940	1100
OSC IN	481	1100
OSC OUT	−102	1100
V_{DD}	0	0
M1	578	0
M2	936	0
STOP	1290	0
chip corner max. value	−470	−160

32 kHz CLOCK CIRCUIT

GENERAL DESCRIPTION

The PCA153X series are silicon-gate CMOS integrated circuits specially suited for battery-operated, quartz-crystal-controlled clocks with a bipolar stepping motor.

Features

- Oscillator frequency 32 kHz
- Low current consumption: typically 2.0 μA, maximum 5 μA
- Low minimum supply voltage: 1.1 V
- Output for bipolar stepping motor
  output frequency: 1 Hz
  pulse duration: see available types
- Test mode speed-up with an input frequency up to 20 Hz (unaltered pulse duration)

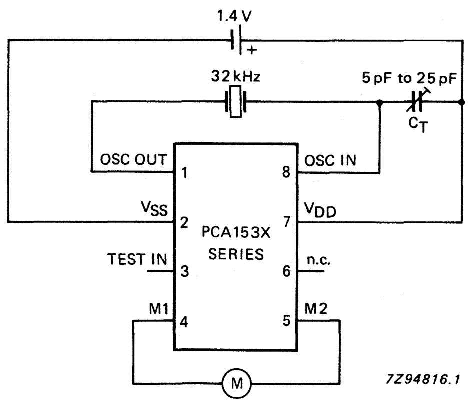


Fig.1 Typical application circuit diagram.

PACKAGE OUTLINES

PCA153XP: 8-lead DIL; plastic (SOT97).
PAC153XT: 8-lead mini-pack; plastic (SO8; SOT96C).
PCA153XU/10: chip-on-film frame carrier (FFC).

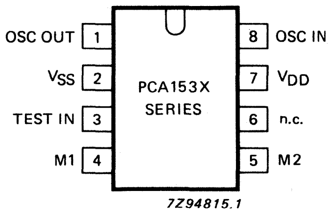


Fig.2 Pinning diagram.

PINNING

1	OSC OUT	oscillator output
2	V_{SS}	GND, 0 V
3	TEST IN	test input
4	M1	motor 1 output
5	M2	motor 2 output
6	n.c.	not connected
7	V_{DD}	supply voltage
8	OSC IN	oscillator input

FUNCTIONAL DESCRIPTION AND TESTING

Operating mode

In the operating mode pin 3 must be left open or connected to V_{DD}.

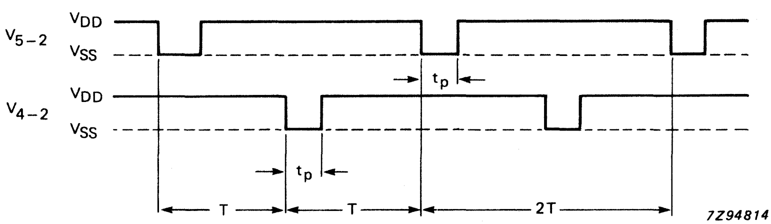


Fig.3 Motor output waveforms.

Test mode

When testing the motor, a test frequency can be applied to TEST IN (pin 3) which allows the motor outputs to be accelerated up to 20 Hz.

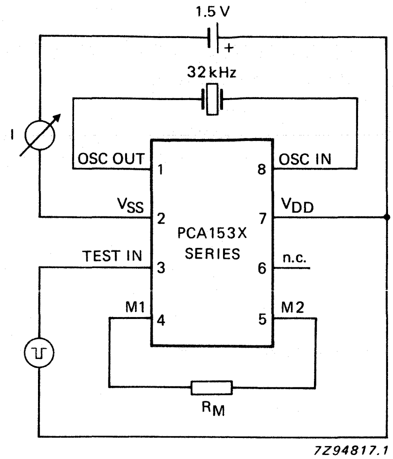


Fig.4 Test speed-up circuit.

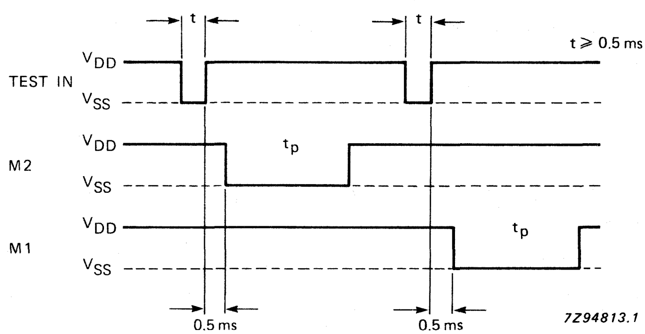


Fig.5 Test speed-up signals.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (V_{DD} = 0 V); note 1	V_{SS}	+ 1.8 to −6 V
Input voltage; note 2	V_I	V_{SS} to V_{DD} V
Output short-circuit duration at pins 4 and 5		indefinite
Operating ambient temperature range	T_{amb}	−10 to + 60 °C
Storage temperature range	T_{stg}	−30 to + 125 °C

Notes

1. Connecting the battery at 1.8 V maximum with reversed polarity does not destroy the circuit, but in this condition a large current flows, which will rapidly discharge the battery.
2. Input and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = −1.4 V; f_{osc} = 32.768 kHz; T_{amb} = 25 °C; R_S = 20 kΩ; crystal: C_1 = 2 to 3 fF; C_o = 1 to 3 pF; C_L = 10 pF; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	operating	V_{SS1}	−1.1	–	−1.8	V
Supply voltage	starting	V_{SS2}	−1.2	–	–	V
Supply current	$R_L = \infty$	I_{DD}	–	2	5	μA
Motor output						
Period		T	–	1.0	–	s
Pulse width		t_p	see available types			ms
Current into load	R_M = 200 Ω; V_{SS} = −1.2 V	I_M	± 4	–	–	mA
Output impedance	R_M = 200 Ω	R_o	–	60	–	Ω
TEST input current	pin 3; TEST = V_{SS}	I_{TEST}	–	70	–	μA
Oscillator						
Polarization resistance		R_p	3	10	30	MΩ
Output capacitance	pin 1; note 1	C_o	see available types			pF
Input capacitance	pin 8; note 1	C_i	see available types			pF
Frequency stability	ΔV_{SS} = 100 mV	Δf/f	–	0.4×10^{-6}	–	

Note to the characteristics

1. Sum of C_i and C_o limited to 40 pF.

AVAILABLE TYPES

Type number	pulse width t_p (ms)	capacitance output C_o (pF)	capacitance input C_i (pF)
PCA1532	23.4	24.0	3.0
PCA1534	46.8	24.0	3.0

CHIP DIMENSIONS AND BONDING PAD LOCATIONS

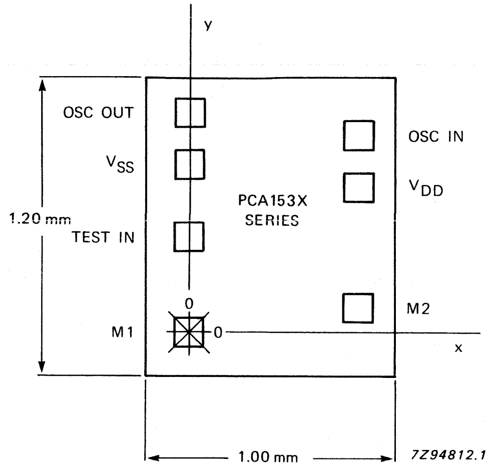


Fig.6 Bonding pad locations; 7 terminals.

Bonding pad dimensions 120 μm x 120 μm
Chip area = 1.20 mm^2

Table 1 Bonding pad locations (dimensions in μm)
All x/y co-ordinates are referenced to the bottom left pad M1, see Fig. 6.

pad	x	y
OSC OUT	0	880
V_{SS}	0	670
TEST IN	0	380
M1	0	0
M2	675	94
V_{DD}	675	575
OSC IN	675	785
chip corner max. value	−180	−180

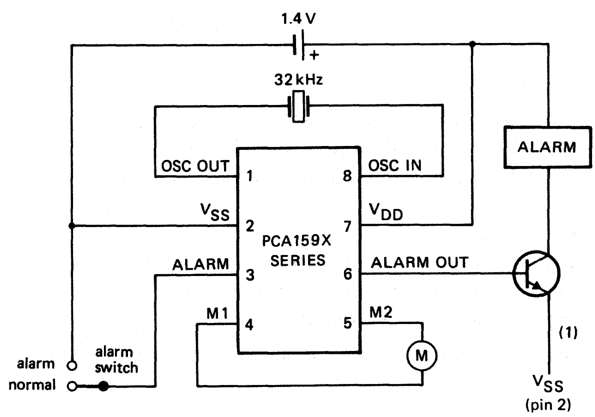
32 kHz ALARM CLOCK CIRCUIT WITH FREQUENCY ADJUSTMENT

GENERAL DESCRIPTION

The PCA159X series are silicon-gate CMOS integrated circuits specially suited for battery-operated, quartz-crystal-controlled clocks with a bipolar stepping motor.

Features

- Oscillator frequency 32 kHz
- Low current consumption: typically 1.5 μA, maximum 5 μA
- Low minimum supply voltage: 1.1 V
- Alarm input
- Motor test
- Test mode speed-up for fast testing
- Quartz frequency electrically programmable and reprogrammable (via EEPROM)
- Protected against electrostatic charges



(1) The emitter of the alarm transistor must be connected to V_{SS}, except when used as a replacement for the PCA158X series where it must be connected to pin 3; in this case the base of the alarm transistor must be connected via a series resistor of 1 kΩ.

Fig.1 Typical application circuit diagram.

PACKAGE OUTLINES

PCA159XP: 8-lead DIL; plastic (SOT97).
PCA159XT: 8-lead mini-pack; plastic (SO8; SOT96C).
PCA159XU/10: chip-on-film frame carrier (FFC).

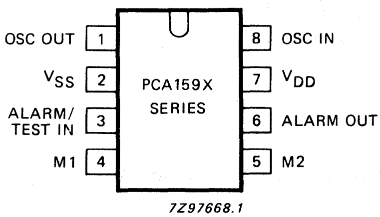


Fig.2 Pinning diagram.

PINNING

1	OSC OUT	oscillator output
2	V_{SS}	GND, 0 V
3	ALARM/ TEST IN	alarm and test input
4	M1	motor 1 output
5	M2	motor 2 output
6	ALARM OUT	alarm output
7	V_{DD}	supply voltage
8	OSC IN	oscillator input

FUNCTIONAL DESCRIPTION AND TESTING

Operating mode

The alarm input (pin 3) is left open. An output frequency of 256 Hz is provided at pin 3 for test purposes.

Alarm mode

The alarm input is connected to V_{SS}. The alarm signal according to Fig. 4 is provided at pin 6.

Test mode

The circuit must be in normal operating mode for at least 10 ms before going into the test mode.
The test mode consists of two parts:

motor test

The alarm input is connected to V_{DD}. In this test mode the motor output period is 125 ms (all types) and the motor pulse width is identical to that of the normal mode. The alarm output periods are also increased by a factor of 128. In addition the alarm modulation is suppressed.

IC test (IC supplier only)

The customer uses this mode during frequency programming. On the negative edge of the first positive pulse (see Fig.8) the IC test is enabled. The motor output is increased by a factor of 1024. The duty factor in this mode is 1:1. The alarm mode is disabled.

On the positive edge of the second pulse (corresponding to the first program pulse) the motor test mode is re-selected.

To disable the test mode, pin 3 must be left open or connected to V_{SS}.

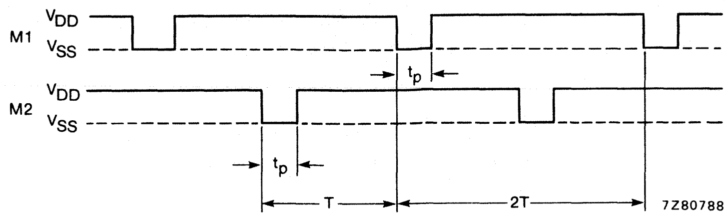


Fig.3 Motor output waveforms.

DEVELOPMENT DATA

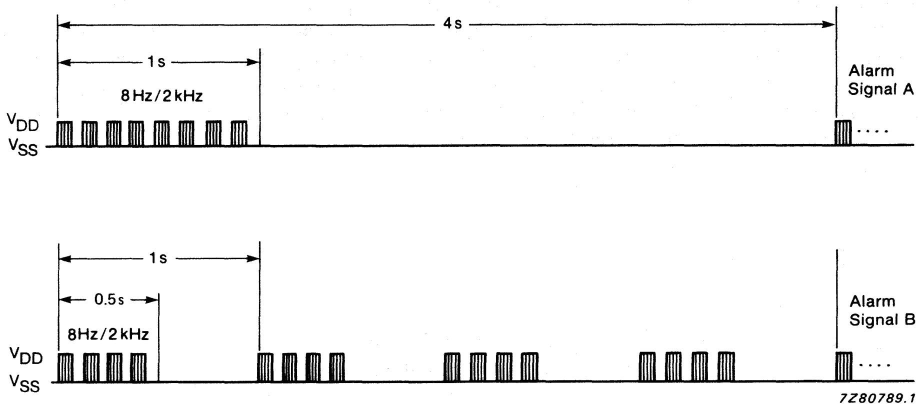


Fig.4 Alarm output waveforms.

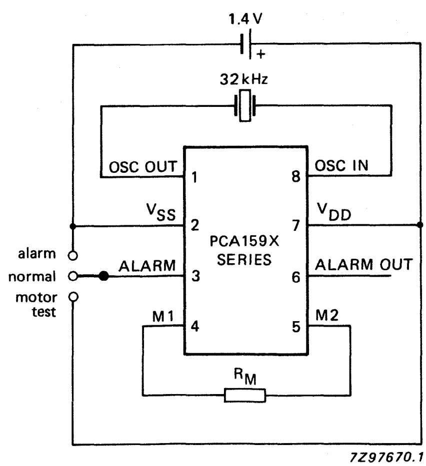


Fig.5 Test and test speed-up circuit.

Frequency trimming

Frequency trimming is carried out by electrically programming the oscillator input capacitance to one of 64 values contained within the non-volatile memory. This is accomplished by carrying out the following five steps; Figs 6, 7, 8 and 9 illustrate this procedure.

1. Erasing

With V_{SS} = −1.4, the generator (pin 3) is taken from −1.4 V to 0 V. The device is now in test mode. Erasure is carried out by increasing V_{SS} to −5.5 V and setting the generator (pin 3) to + 1.4 V.

2. Checking erasing/zero

With V_{SS} = −1.4 V, the generator (pin 3) is taken from −1.4 V to 0 V. The device is in test mode and the minimum capacitance is obtained.

3. Measure/data input

On the first 1.4 V pulse (pin 3) the test mode is changed from motor test to IC test. This pulse releases the program register thus allowing the frequency to be programmed. The positive edge of the second pulse switches the IC test mode back to the motor test mode. The negative edge of the second pulse increases the capacitance by one unit, this happens on all the subsequent pulses. The frequency can be measured between these increases. This procedure is repeated until the required frequency is obtained. If the adjustment to the frequency is greater than required, the procedure can be restarted with step 2.

4. Writing

The capacitance is fixed by increasing V_{SS} to −5.5 V.

5. Checking writing

With V_{SS} = −1.4 V, the generator (pin 3) is taken from −1.4 V to 0 V. The device is in test mode and the trimmed capacitance is obtained. The frequency can be checked.

Note

The information concerning the capacitive value is obtained from the EEPROM cells and the program register. Therefore the program register must be reset before the frequency can be measured (see steps 1 to 5). Programming can be performed 10 times.

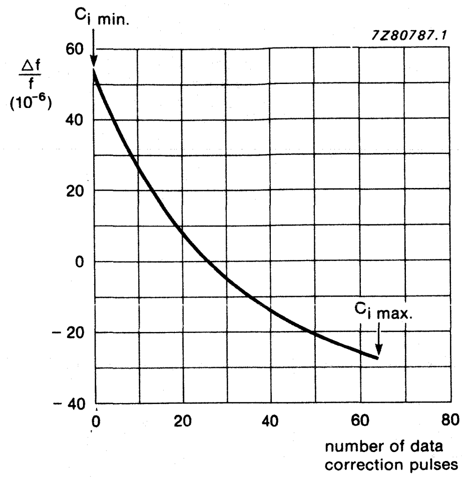
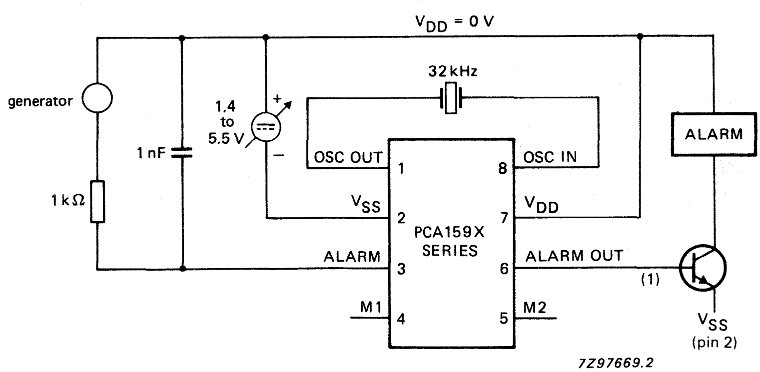


Fig.6 Typical frequency characteristic.
C_1 = 2.8 fF; C_0 = 3 pF; C_L = 10 pF;
f = 32.768 kHz.

DEVELOPMENT DATA



(1) During programming ALARM OUT is active LOW, so that programming is possible when the alarm transistor is connected to pin 6.

Fig.7 Frequency trimming circuit.

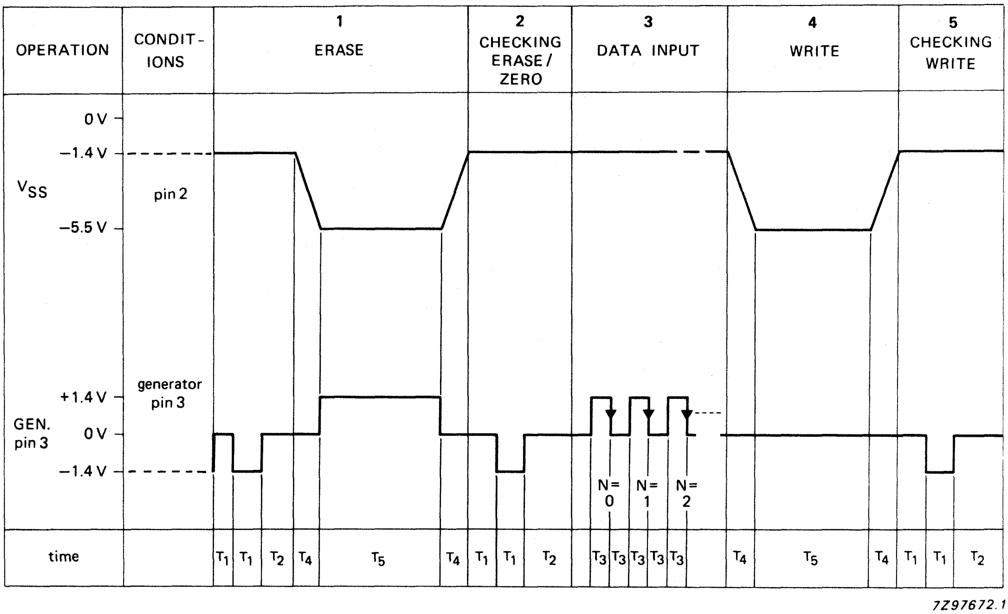


Fig.8 Frequency trimming signals (V_{DD} = 0 V).

Table 1 Frequency trimming timing requirements

time	symbol	min.	max.	units
Reset time 1	T_1	1	–	ms
Reset time 2	T_2	5	–	ms
Data pulse width/gap	T_3	100	–	μs
Supply rise/fall time	T_4	1	–	ms
WRITE/ERASE time	T_5	10	–	ms

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (V_{DD} = 0 V); note 1	V_{SS}	+ 1.8 to −6 V
Input voltage (on all pins except pin 3); note 2	V_I	V_{SS} to V_{DD} V
Input voltage at pin 3	$V_{3\text{-}2}$	V_{SS} to V_{DD} + 1 V
Output short-circuit duration at pins 4, 5 and 6		indefinite
Operating ambient temperature range	T_{amb}	−10 to + 60 °C
Storage temperature range	T_{stg}	−30 to + 125 °C
Resistance against electrostatic discharge		note 3

Notes

1. Connecting the battery at 1.8 V maximum with reversed polarity does not destroy the circuit, but in this condition a large current flows, which will rapidly discharge the battery.
2. Input and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').
3. Three discharges of a 100 pF capacitor at 800 V, through a resistor of 1.5 kΩ (with positive and negative polarity).

AVAILABLE TYPES

	motor output			
	period	pulse width	minimum current	alarm signal (see Fig.4)
Type number	T (s)	t_p (ms)	I_M (mA)	
PCA1593	1	31.25	4.3	B
PCA1594	1	46.8	4.3	A
PCA1595	1	46.8	4.3	B
PCA1596	1	15.6	4.3	A
PCA1597	4	15.6	4.3	B

CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = −1.4 V; f_{osc} = 32.768 kHz; T_{amb} = 25 °C; R_S = 20 kΩ; crystal: C_1 = 2 to 3 fF; C_o = 3 pF; C_L = 10 pF; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	operating	V_{SS1}	−1.1	−	−1.8	V
Supply voltage	starting	V_{SS2}	−1.2	−	−	V
Supply voltage	programming	V_{SS3}	−5.4	−5.5	−5.6	V
Supply current	$R_L = \infty$	I_{DD}	−	1.5	5.0	μA
Motor output						
Period	see available types for the typical value	T	1.0	−	60.0	s
Pulse width	see available types for the typical value	t_p	3.9	−	62.5	ms
Current into load	R_M = 200 Ω; V_{SS} = −1.2 V	I_M	4.3	−	−	mA
Output impedance	R_M = 200 Ω	R_o	−	50	−	Ω
Alarm output						
Output waveform			see Fig. 4			
Sink current	R = 10 kΩ; V_{SS} = −5.5 V	I_6	−	200	−	μA
Source current	R = 1 kΩ; V_{SS} = −1.2 V	I_6	0.3	1	−	mA
Alarm test input						
Delay			−	−	70	ms
Input current	note 1	I_3	−	2	−	μA
Input current	note 1; V_{SS} = −5.5 V	I_3	−	50	−	μA
Oscillator						
Polarization resistance		R_p	3	10	30	MΩ
Output capacitance	pin 1	C_0	−	24	−	pF
Input capacitance data pulses	pin 8; n = 0; note 2	C_I	−	9	−	pF
Input capacitance steps		ΔC	−	0.25	−	pF
Frequency stability	ΔV_{SS} = 100 mV; n = 20	Δf/f	−	0.6×10^{-6}	−	
Data retention time	T_{amb} = −10 to +60 °C	T_{ret}	−	10	−	years

Notes to characteristics

1. These values are averages for the 256 Hz output with 1: 1 duty factor.
2. Number of data correction pulses (n).

CHIP DIMENSIONS AND BONDING PAD LOCATIONS

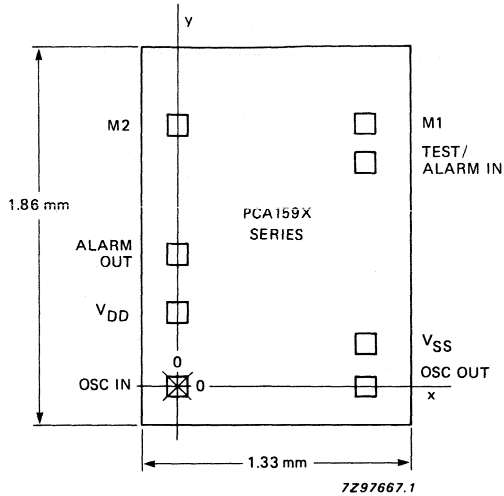


Fig.9 Bonding pad locations.

Bonding pad dimensions 110 μm x 110 μm
Chip area = 2,47 mm^2

Table 2 Bonding pad locations (dimensions in μm)
All x, y co-ordinates are referenced to the bottom left pad (OSC IN), see Fig.9.

pad	x	y
OSC OUT	1006	0
V_{SS}	1006	220
TEST/ALARM IN	1006	1111
M1	1006	1296
M2	0	1296
ALARM OUT	0	651
V_{DD}	0	376
OSC IN	0	0
chip corner max. value	−192	−190

DEVELOPMENT DATA

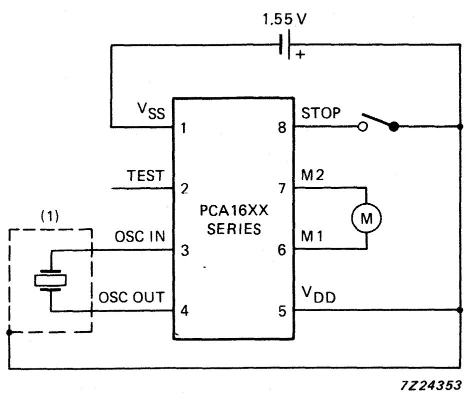
32 kHz WATCH CIRCUIT WITH EEPROM

GENERAL DESCRIPTION

The PCA16XX series are CMOS integrated circuits specially suited for battery-operated, quartz-crystal-controlled wrist-watches, with bipolar stepping motors.

Features

- 32 kHz oscillator, amplitude regulated with excellent frequency stability
- Oscillator with high immunity to leakage currents
- Electrically programmable/reprogrammable timekeeping adjustment (via EEPROM)
- Requires only one external component: quartz crystal
- Very low current consumption: typically 170 nA
- Detector for silver oxide or lithium battery voltage levels
- Battery end-of-life indicator
- Stop function for accurate timing
- Power-ON reset for fast testing
- Separate test modes for testing the mechanical parts of the watch and the IC



(1) Case to be connected to V_{DD}. Stray capacitance and leakage resistance from RESET, M1 or M2 to OSC IN should be less than 0.5 pF or larger than 20 MΩ respectively.

Fig.1 Typical application circuit diagram.

PACKAGE OUTLINES

PCA16XXT; 8-lead micro flat-pack; plastic (SOT144).
PCA16XXU; chip in tray.

PINNING

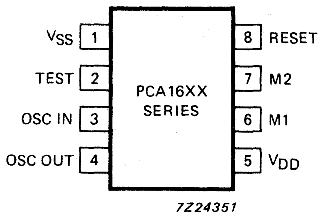


Fig.2 Pinning diagram.

1	V_{SS}	ground (0 V)
2	TEST	test input
3	OSC IN	oscillator input
4	OSC OUT	oscillator output
5	V_{DD}	positive supply voltage
6	M1	motor output 1
7	M2	motor output 2
8	RESET	reset input

GENERAL DESCRIPTION

Motor pulse

The motor pulse widths (t_W) and the cycle times (t_T) are given in Table 2.

Voltage level detector

The supply voltage is compared with the internal reference voltage V_{LIT} and V_{EOL} every minute. The first voltage level detection is performed 30 ms after a RESET.

Lithium mode

If a lithium voltage level is detected ($V_{DD} \geqslant V_{LIT}$), the circuit will operate in the lithium mode. The motor pulse will be produced with a 75% duty factor.

Silver oxide mode

If the voltage level detected is between V_{LIT} and V_{EOL}, the circuit will operate in silver oxide mode. The motor pulse will be produced without chopping.

Battery-end-of-life *

If the battery end-of-life is detected ($V_{DD} \leqslant V_{EOL}$), the motor pulse will be produced without chopping. To indicate this condition, bursts of 4 pulses are produced every 4 s.

Power-ON reset

For correct operation of the power-ON reset the rise time of V_{DD}, from 0 V to 2.1 V, should be less than 0.1 ms. All resetable flip-flops are reset. The first motor pulse is always positive after a power-ON reset ($V_{M1} - V_{M2} \geqslant 0$ V).

* Only available for types with a 1 s motor pulse.

Customer testing

An output frequency of 32 Hz is provided at RESET for exact frequency measurement. Every minute a jitter occurs as a result of timekeeping adjustment, which occurs 90 to 150 ms after disconnecting RESET from V_{DD}.

Connecting pin RESET to V_{DD} stops the motor pulse signals (leaving them in a HIGH impedance, 3-state condition) and produces a jitter-free 32 Hz signal at the TEST pin. A debounce circuit protects against accidental stoppages due to mechanical shock to the watch (t_{DEB} = 13.7 to 78.1 ms).

Connecting RESET to V_{SS} activates Tests 1 and 2 and disables the timekeeping adjustment.

In Test 1 ($V_{DD} > V_{EOL}$) normal function takes place except the voltage detection cycle (t_V) is 125 ms and the cycle time is t_{T1}. At pin TEST a minute signal is available at 8192 times it normal frequency.

In Test 2* ($V_{DD} < V_{EOL}$) the voltage detection cycle (t_V) is 31.25 ms and the motor pulse period (t_{T2}) = 31.25 ms.

Test and reset mode are terminated by disconnecting the RESET pin.

Test 3: if V_{DD} voltage level is greater than 5 V, motor pulses with a time period of t_{T3} = 31.25 ms + n x 122 μs are produced to check the contents of the EEPROM. At pin TEST the motor pulse period signal (t_T) is available at 1024 times it normal frequency. The circuit returns to normal operation when $V_{DD} < 2.5$ V between two motor pulses.

Timekeeping adjustment**

To compensate for the tolerance of the quartz crystal frequency, a number (n) of 8192 Hz pulses are inhibited every minute of operation. The number (n) is stored in a non-volatile memory, the EEPROM, which is achieved by the following steps (see Fig.4):

1. The quartz frequency deviation ($\Delta f/f$) and n are found from the information supplied in Table 1.
2. V_{DD} is increased to 5.1 V. This allows the contents of the EEPROM to be checked, as described in step 9.
3. V_{DD} is decreased to 2.5 V during a motor pulse to initialize a storing sequence.
4. The first V_{DD} pulse to 5.1 V erases the contents of EEPROM.
5. When the EEPROM is erased a logic 1 is present on pin TEST.
6. V_{DD} is increased to 5.1 V to start the data input sequence. V_{DD} is pulsed n times to 4.5 V until the required value is obtained. After the value is obtained V_{DD} is decreased to 2.5 V.
7. V_{DD} is increased to 5.1 V to store the data in the EEPROM and reset the circuit.
8. V_{DD} is decreased to the operating voltage level to terminate the storing sequence and to turn to operating mode.
9. V_{DD} is increased to 5.1 V to check the timekeeping adjustment.
   Timekeeping adjustment is checked by measuring the motor pulse period (t_{T3}).
10. V_{DD} is decreased to the operating voltage between two motor pulses to return to operating mode.

* Only applicable for types with the battery end-of-life detector.

** Programming can be performed ten times.

Table 1 Quartz crystal frequency deviation and n

$\frac{\Delta f}{f} \times 10^{-6}$ (ppm)	n	t_{T3} step 2 or 9 (ms)
2.03	1	31.372
4.06	2	31.494
.	.	.
.	.	.
127.89	63	38.936

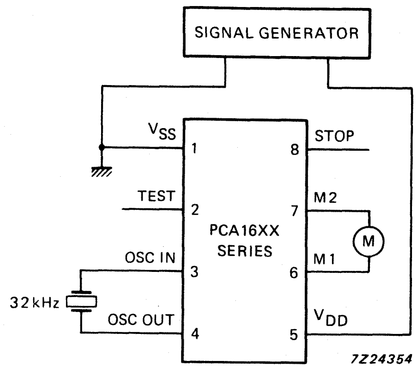
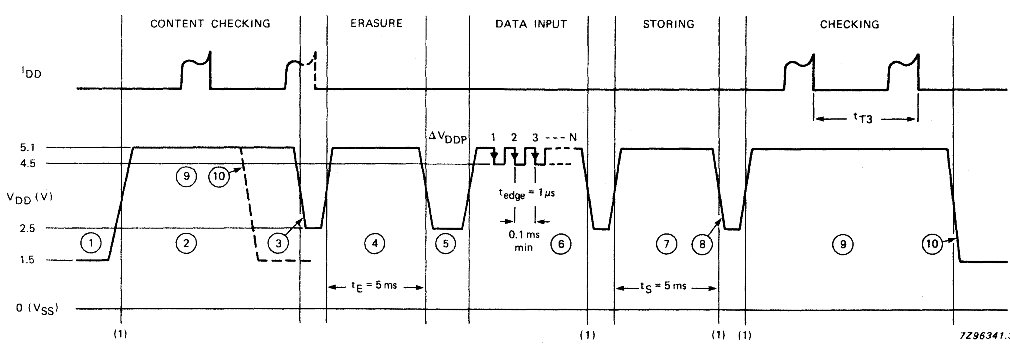


Fig. 3 Programming circuit diagram.



(1) Rise and fall times should be greater than 1 ms to allow instaneous and accurate checking.

Fig.4 Timekeeping adjustment programming.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	note 1	V_{DD}	−1.8	6.0	V
All input voltages	note 2	V_I	V_{SS}	V_{DD}	V
Output short-circuit duration		t_{sc}	indefinite		
Operating ambient temperature range		T_{amb}	−10	+60	°C
Storage temperature range		T_{stg}	−30	+100	°C
Electrostatic handling	note 3	V_{es}	−800	+800	V

Notes to the ratings

1. V_{SS} = 0 V. Connecting the battery with reversed polarity does not destroy the circuit, but in this condition a large current flows, which will rapidly discharge the battery.
2. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices (see 'Handling MOS Devices').
3. Equivalent to three discharges of a 100 pF capacitor at 800 V, through a resistor of 1.5 kΩ (with positive and negative polarity).

CHARACTERISTICS (note 1)

V_{DD} = 1.55 V; V_{SS} = 0 V; crystal: R_S = 20 kΩ; C_L = 8 pF to 10 pF; f_{osc} = 32768 Hz; C1 = 2 fF to 3 fF; C_0 = 1 pF to 3 pF; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	T_{amb} = −10 °C to +60 °C	V_{DD}	1.2	1.5	2.5	V
Acceptable supply voltage transient	V_{DD} = 1.2 V to 2.5 V	ΔV_{DD}	–	–	0.25	V
Programming voltage		V_{DDP}	5.0	5.1	5.2	V
Programming pulse voltage		ΔV_{DDP}	0.55	0.60	0.65	V
Supply current	between motor pulses	I_{DD1}	–	170	260	nA
	between motor pulses; V_{DD} = 2.1 V	I_{DD2}	–	190	300	nA
	Stop mode; pin 8 connected to V_{DD}	I_{DD3}	–	180	280	nA
	Stop mode; pin 8 connected to V_{DD}; V_{DD} = 2.1 V	I_{DD4}	–	220	360	nA
	T_{amb} = −10 °C to +60 °C; V_{DD} = 2.1 V	I_{DD5}	–	–	600	nA
Motor outputs						
Saturation voltage $\Sigma(P + N)$	R_L = 2 kΩ; T_{amb} = −10 °C to 60 °C	V_{SAT}	–	150	200	mV
Short-circuit resistance $\Sigma(P + N)$	$I_{transistor}$ < 1 mA	R_{sc}	–	200	300	Ω
Cycle time		t_T		note 2		s
Pulse width		t_P		note 3		ms
Voltage level detector						
Threshold voltage	lithium mode	V_{LIT}	1.65	1.80	1.95	V
	battery end-of-life	V_{EOL}	1.27	1.38	1.46	V
Threshold hysteresis		ΔV_{VLD}	–	10	–	mV
Temperature coefficient		ΔV_{VLD}/°C	–	−1	–	mV/°C
Voltage detection cycle		t_V	–	60	–	s

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Start-up voltage		V_{OSC}	1.2	–	–	V
Transconductance	$V_{i(p-p)} \leqslant 50$ mV	g_m	6	15	–	µA/V
Frequency stability	ΔV_{DD} = 100 mV	$\Delta f/f$	–	0.05	0.3	10^{-6}
Input capacitance		C_I	8	10	12	pF
Output capacitance		C_O	12	15	18	pF
Start-up time		t_{OSC}	–	1	–	s
Reset input						
Output frequency		f_o	–	32	–	Hz
Output voltage swing	R = 1 MΩ; C = 10 pF	ΔV_o	1.4	–	–	V
Edge time	R = 1 MΩ; C = 10 pF	t_{edge}	–	1	–	µs
Peak input current	note 4	I_{im}	–	320	–	nA
Average input current		$I_{i(av)}$	–	10	–	nA
Test input						
Pulse width	TEST 1	t_{T1}	see Table 2			
	TEST 2	t_{T2}	–	31.25	–	ms
	TEST 3	t_{T3}	see Table 1			
Debounce time	RESET = V_{DD}	t_{DEB}	13.7	–	78	ms
Battery end-of-life						
End-of-life sequence		t_{EOL}	–	4	–	s
Motor pulse width	see Table 2	t_{E1}	–	t_p	–	ms
Time between pulses		t_{E2}	–	31.25	–	ms

Notes to the characteristics

1. Immunity against parasitic impedance (pin to adjacent pin) = 20 MΩ.
2. Cycle time can be changed to one of the following values 1, 5, 10, 12 or 20 ms. See Table 1.
3. Pulse width can be varied from 2 ms to 15.7 ms (in steps of 1 ms). See Table 1.
4. Duty factor = 1 : 32 and RESET connected to V_{DD} or V_{SS}.

Table 2 Available types and timing information (see Fig.5)

type no.	pulse width t_P (ms)*	cycle time normal mode t_T (s)**	test mode t_{T1} (ms)	modes lithium	silver	end-of-life	remarks
PCA1601	7.81	1	31.25	–	●	–	–
PCA1602	7.81	1	31.25	–	●	–	75% chopped
PCA1605	4.80	20	31.25	–	●	–	–
PCA1606	6.80	10	31.25	–	●	–	–
PCA1609	5.80	1	31.25	–	●	–	–

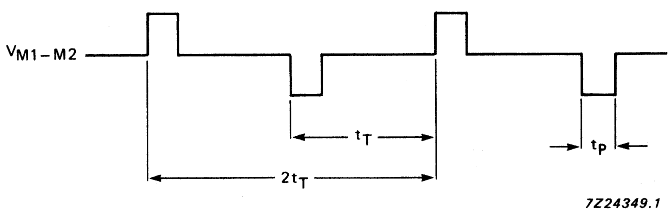


Fig.5 Motor output waveform (normal operation).

* See note 3 to the characteristics.
** See note 2 to the characteristics.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS

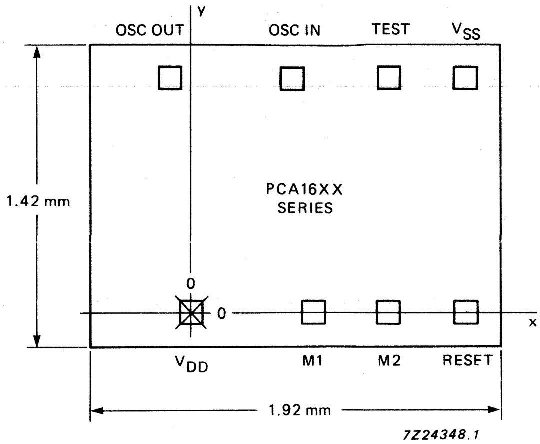


Fig.6 Bonding pad locations.

DEVELOPMENT DATA

Bonding pad dimensions 110 μm x 110 μm
Chip area = 2.73 mm^2

Table 2 Bonding pad locations (dimensions in μm)

All x, y co-ordinates are referenced to the center of pad V_{DD}, see Fig.6.

pad	x	y
V_{SS}	1290	1100
TEST	940	1100
OSC IN	481	1100
OSC OUT	−102	1100
V_{DD}	0	0
M1	578	0
M2	936	0
RESET	1290	0
chip corner	−470	−160

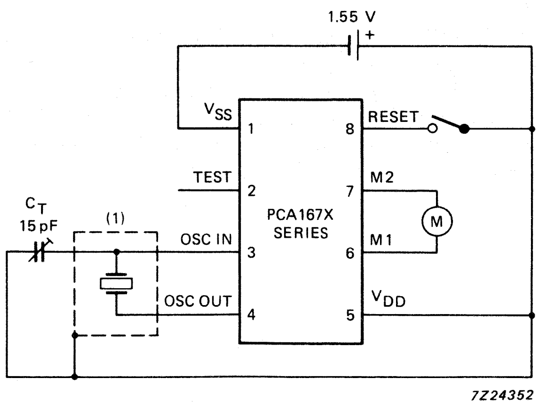
32 kHz WATCH CIRCUIT USING A SILVER OXIDE OR A 3 V LITHIUM BATTERY

GENERAL DESCRIPTION

The PCA167X series are CMOS integrated circuit specially suited for battery-operated, quartz-crystal-controlled wrist-watches, with a bipolar stepping motor.

Features

- 32 kHz oscillator, amplitude regulated with excellent frequency stability
- Oscillator with high immunity to leakage currents
- Very low current consumption: typically 150 nA
- Stop function for accurate timing
- Separate test modes for testing the mechanical parts of the watch and the IC
- Chopped motor pulses available
- Power-on reset for fast testing



(1) Case to be connected to V_{DD}. Stray capacitance and leakage resistance from RESET, M1 or M2 to OSC IN should be less than 0.5 pF or larger than 20 MΩ respectively.

Fig.1 Typical application circuit diagram.

PACKAGE OUTLINES

PCA167XT; 8-lead micro flat-pack; plastic (SOT144).
PCA167XU; chip in tray.

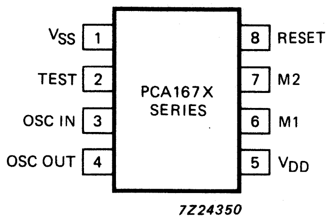


Fig.2 Pinning diagram.

PINNING

1	V_{SS}	ground (0 V)
2	TEST	test input
3	OSC IN	oscillator input
4	OSC OUT	oscillator output
5	V_{DD}	positive supply voltage
6	M1	motor output 1
7	M2	motor output 2
8	RESET	reset input

GENERAL DESCRIPTION

Motor pulse

The motor output pulse widths (t_p) and the cycle times (t_T) for each type are given in Table 1.

Power-ON reset

For correct operation of the power-ON reset , the rise time of V_{DD} (from 0 V to 1.55 V) should be less than 0.1 ms. All resetable flip-flops are reset. The first motor pulse is always positive after a power-ON reset ($V_{M1} - V_{M2} \geqslant 0$ V).

Customer testing and stop mode

An output frequency of 32 Hz is available at RESET (pin 8) for exact frequency measurement. Connecting the RESET pin to V_{DD} stops the motor pulse signals (leaving them in a HIGH impedance, 3-state condition) and produces a 32 Hz signal at the TEST pin. A debounce circuit protects against accidental stoppages due to mechanical shock to the watch (t_{DEB} = 13.7 to 78.1 ms). Connecting RESET to V_{SS} activates the test mode. The motor pulse period is 31.25 ms instead of t_T. Test and stop mode are disabled by disconnecting RESET (open-circuit).

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	see note 1	V_{DD}	−1.8	6.0	V
All input voltages	see note 2	V_I	V_{SS}	V_{DD}	V
Output short-circuit duration		t_{sc}	indefinite		
Operating ambient temperature range		T_{amb}	−10	+ 60	°C
Storage temperature range		T_{stg}	−30	+ 100	°C
Electrostatic handling	see note 3	V_{es}	−800	+ 800	V

Notes to the ratings

1. V_{SS} = 0 V. Connecting the battery with reversed polarity does not destroy the circuit, but in this condition a large current flows, which will rapidly discharge the battery.
2. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices (see 'Handling MOS Devices').
3. Equivalent to three discharges of a 100 pF capacitor at 800 V, through a resistor of 1.5 kΩ (with positive and negative polarity).

CHARACTERISTICS

V_{DD} = 1.55 V; V_{SS} = 0 V; crystal: R = 20 kΩ; C_L = 8 pF to 10 pF; f_{osc} = 32768 Hz; C1 = 2 fF to 3 fF; C_0 = 1 pF to 3 pF; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	T_{amb} = −10 °C to + 60 °C	V_{DD}	1.2	1.5	3.5	V
Acceptable supply voltage transient	V_{DD} = 1.2 V to 3.5 V	ΔV_{DD}	–	–	0.25	V
Supply current	between motor pulses	I_{DD1}	–	150	250	nA
	between motor pulses; V_{DD} = 3.5 V	I_{DD2}	–	200	350	nA
	stop mode; pin 8 connected to V_{DD}	I_{DD3}	–	180	300	nA
	stop mode; pin 8 connected to V_{DD}; V_{DD} = 3.5 V	I_{DD4}	–	300	480	nA
Motor outputs						
Saturation voltage Σ(P + N)	R_L = 2 kΩ; T_{amb} = −10 °C to 60 °C	V_{SAT}	–	150	200	mV
Short-circuit resistance Σ(P + N)	$I_{transistor}$ < 1 mA	R_{sc}	–	200	300	Ω
Cycle time		t_T		note 1		s
Pulse width		t_p		note 2		ms
Oscillator						
Start-up voltage		V_{OSC}	1.2	–	–	V
Transconductance	$V_{i(p-p)}$ = 50 mV	g_m	6	15	–	μS
Frequency stability	ΔV_{DD} = 100 mV	Δf/f	–	0.05	0.3	10^{-6}
Input capacitance		C_I	–	3	–	pF
Output capacitance		C_O	19	24	29	pF
Start-up time		t_{OSC}	–	1	–	s
Reset input						
Output frequency		f_o	–	32	–	Hz
Output voltage swing	R = 1 MΩ; C = 10 pF	ΔV_o	1.4	–	–	V
Edge time	R = 1 MΩ; C = 10 pF	t_{edge}	–	1	–	μs
Peak input current	see note 3	I_{im}	–	320	–	nA
Average input current		$I_{i(av)}$	–	10	–	nA
Test input						
Pulse width		t_{T1}		see Table 1		
Debounce time	RESET = V_{DD}	t_{DEB}	13.7	–	78	ms

Notes to the characteristics

1. Cycle time can be changed to one of the following values 1, 5, 10, 12 or 20 ms. See Table 1.
2. Pulse width can be varied from 2 ms to 15.7 ms (in steps of 1 ms). See Table 1.
3. Duty factor = 1:32 and RESET connected to V_{DD} or V_{SS}.

Table 1 Available types and timing information

type no.	pulse width t_p (ms)	cycle time		battery type		remarks
		normal mode t_T (s)	test mode t_{T1} (s)	silver	lithium	
PCA1671	7.81	1	31.25	•	–	–
PCA1672	7.81	1	31.25	–	•	56% chopped (1 kHz)
PCA1674	7.81	5	31.25	•	–	–
PCA1678	5.80	20	31.25	•	–	–

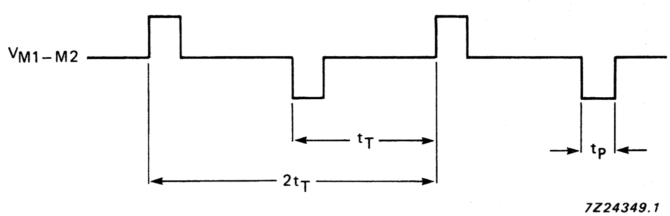


Fig.3 Motor output waveform (normal operation).

CHIP DIMENSIONS AND BONDING PAD LOCATIONS

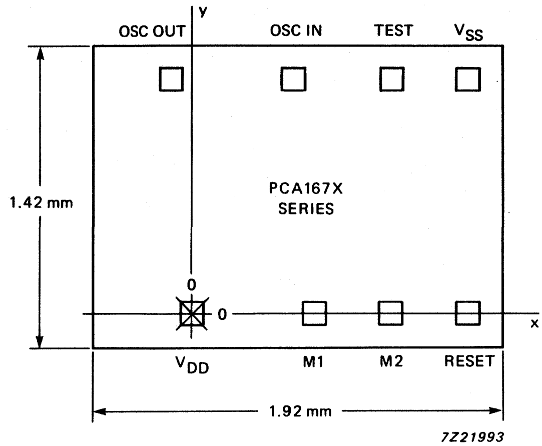


Fig.4 Bonding pad locations.

Bonding pad dimensions 110 μm x 110 μm
Chip area = 2.73 mm^2

Table 2 Bonding pad locations (dimensions in μm
All x, y co-ordinates are referenced to the center of pad V_{DD}, see Fig.4.

pad	x	y
V_{SS}	1290	1100
TEST	940	1100
OSC IN	481	1100
OSC OUT	–102	1100
V_{DD}	0	0
M1	578	0
M2	936	0
RESET	1290	0
chip corner	–470	–160

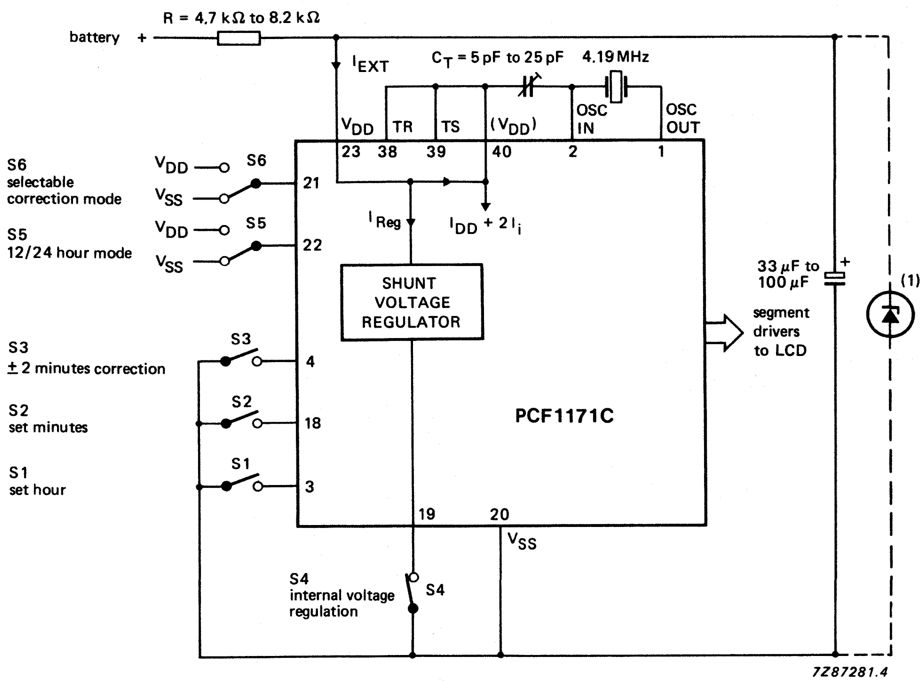
4-DIGIT LCD CAR CLOCK

GENERAL DESCRIPTION

The PCF1171C is a single chip, 4.19 MHz CMOS clock circuit indicating hours and minutes. It is designed to drive a 3½ or 4-digit liquid crystal display (LCD). Two single-pole, single-throw switches accomplish all time setting functions. A bonding option allows the selection of 12-hour or 24-hour display mode. The circuit is battery operated via an internal 5 V voltage regulator or by an external stabilized voltage supply.

Features

- Driving standard 3½ or a 4-digit LCD
- Internal voltage regulator for 5 V LCD
- Option for external stabilized voltage supply
- 4,19 MHz oscillator
- Integrated oscillator output capacitor and polarization resistor
- Operating ambient temperature range –40 to +85 °C
- 40-lead plastic mini-pack (VSO40)



(1) Only needed if internal regulation is disconnected.

Fig. 1 Typical application diagram.

Note: From pin 2 (OSC IN) to any other pin the stray capacitance should not exceed 2 pF.

PACKAGE OUTLINES

PCF1171CT: 40-lead mini-pack; plastic (opposite bent leads) (VSO40; SOT158B).
PCF1171CU: uncased chip in tray.

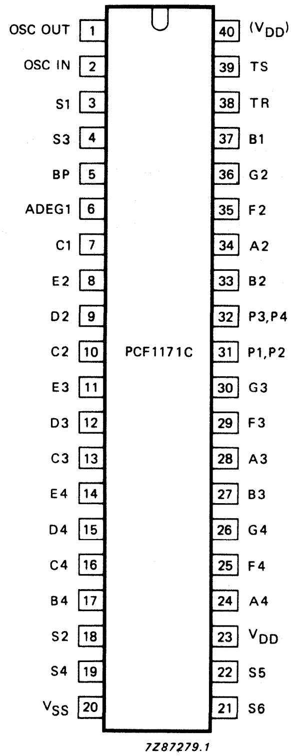


Fig. 2 Pinning diagram.

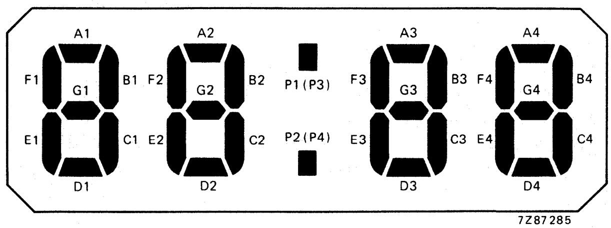


Fig. 3 Segment designation of LCD.

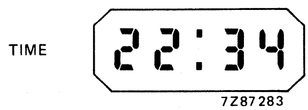


Fig. 4 Display mode.

PINNING

Pin	Symbol	Description
1	OSC OUT	oscillator output
2	OSC IN	oscillator input
3	S1	set hour
4	S3	± 2 minute correction
5	BP	64 Hz backplane driver (common of LCD)
6	ADEG1	segment drivers
7	C1	segment drivers
8	E2	segment drivers
9	D2	segment drivers
10	C2	segment drivers
11	E3	segment drivers
12	D3	segment drivers
13	C3	segment drivers
14	E4	segment drivers
15	D4	segment drivers
16	C4	segment drivers
17	B4	segment drivers
18	S2	set minutes
19	S4	internal voltage regulation
20	V_{SS}	negative supply
21	S6	selectable correction mode
22	S5	12/24-hour mode
23	V_{DD}	positive supply
24	A4	segment drivers
25	F4	segment drivers
26	G4	segment drivers
27	B3	segment drivers
28	A3	segment drivers
29	F3	segment drivers
30	G3	segment drivers
31	P1, P2	colon flashing
32	P3, P4	colon static
33	B2	segment drivers
34	A2	segment drivers
35	F2	segment drivers
36	G2	segment drivers
37	B1	segment drivers
38	TR	test reset; connect to (V_{DD})
39	TS	test speed-up; connect to (V_{DD})
40	(V_{DD})	positive supply for test and oscillator inputs

SWITCH FUNCTIONS

Time set mode

Switch inputs S1, S2 and S3 have an internal pull-up resistor to facilitate use of single-pole, single-throw contacts. A specific debounce circuit is integrated as protection against contact debounce and parasitic voltages.

Switch S1

Set hours, S6 selects mode of correction.

Switch S2

Set minutes, S6 selects mode of correction. When S2 is closed, in addition to the minute correction, the second counter is set to zero. Release of S2 sets the second counter running.

Switches S1 and S2

Segment test: If S1 and S2 are pressed simultaneously all LCD segments are switched on. When the switches are released, the clock starts at 1 : 00 in the 12-hour mode or 0 : 00 in the 24-hour mode.

Switch options

Switch S3

Time correction ± 2 minutes, only operates between 58 minutes 00 seconds and 1 minute 59 seconds. By pressing S3 the clock resets to the full hour with minutes and seconds at zero.

Switch S4

Internal regulation: S4 is closed; the internal voltage regulator is active and the voltage supply for the LCD is 5 V.
External regulation: S4 is open; the circuit has to be supplied with an externally regulated voltage.

Switch S5

12-hour display mode: S5 is connected to V_{DD} for 12-hour operation.
24-hour display mode: S5 is connected to V_{SS} for 24-hour operation.

Switch S6

Single set correction mode: S6 is connected to V_{DD}; each closure of S1 or S2 advances the counter by one.
Continuous set correction mode: S6 is connected to V_{SS}; each closure of S1 or S2 advances the counter by one and after one second continues with one advance per second until S1 or S2 is released.

Testing

In normal operation the test inputs TR (pin 38) and TS (pin 39) have to be connected to V_{DD} (pin 23). A test frequency (64 Hz) is available at BP (pin 5). The test mode is activated by connecting TS to V_{SS} (pin 20). All output frequencies are then increased by a factor of 65 536. In this mode the maximum input frequency is 100 kHz (external generator at OSC_{IN}). By connecting TR to V_{SS} all counters (seconds, minutes and hours) are stopped. After connecting TR to V_{DD} all counters start from an initial state.

Switch functions also operate in the test mode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage with respect to V_{SS} with internal regulation disconnected *	V_{DD}	max.	8 V
Voltage range (any pin)	V_{n-20}		V_{SS} −0.3 to V_{DD} + 0.3 V
Storage temperature range	T_{stg}		−55 to +125 °C
Operating ambient temperature range	T_{amb}		−40 to +85 °C

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; crystal: f = 4.194304 MHz, R_s = 50 Ω, C_L = 12 pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (external regulation)	V_{DD}	3	–	6	V
Supply voltage (internal reg. I_{REG} = 1 mA)	V_{DD}	4	5	6	V
Regulation current (with internal regulation)	I_{REG}	0.2	–	5	mA
Current consumption all switches open; without LCD; internal regulation disconnected; note 1	I_{DD}	50	400	700	μA
Differential internal impedance at I_{REG} = 1 mA	r_o	–	–	150	Ω
Oscillator (pins 1 and 2); note 2					
start time	t_{osc}	–	–	200	ms
frequency stability at ΔV_{DD} = 100 mV	$\Delta f/f_{osc}$	–	0.2×10^{-6}	1×10^{-6}	
feedback resistance	R_{fb}	0.1	–	1	MΩ
input capacitance	C_i	–	–	9	pF
output capacitance	C_o	19	24	29	pF
Switches S1, S2 and S3 (pins 18, 3 and 4) and test inputs, TS, TR (pins 38, 39) output current with inputs connected to to V_{SS}	I_i	50	150	500	μA
debounce time	t_d	32	–	150	ms
Segment driver output resistance at $\pm I_L$ = 50 μA	R_S	–	1	2.5	kΩ
Backplane driver output resistance at $\pm I_L$ = 250 μA	R_{BP}	–	0.2	0.5	kΩ
Backplane driver output frequency	f_{BP}	–	64	–	Hz
LCD DC offset voltage at R_L = 200 kΩ; C_L = 1 nF		–	–	±50	mV

Notes to characteristics

1. The current $I_{EXT} = I_{REG} + I_{DD} + 2 \times I_i$ (+ LCD current).
2. For correct operation of the oscillator: $V_{DD} \geqslant 3$ V.

* Connecting the supply voltage with reverse polarity, will not harm the circuit, provided the current is limited to 10 mA by the external resistor.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS

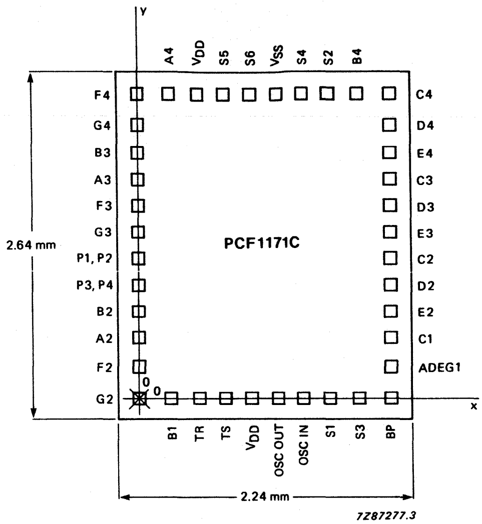


Fig. 5 Bonding pad locations; 40 terminals.

Bonding pad dimensions 110 μm x 110 μm
Chip area = 5.91 mm^2

Table 1 Bonding pad locations (dimensions in μm)
All x/y co-ordinates are referenced to the pad G2; see Fig. 5.

pad	x	y	pad	x	y
OSC OUT	1060	0	S6	860	2320
OSC IN	1260	0	S5	660	2320
S1	1460	0	V_{DD}	460	2320
S3	1680	0	A4	240	2320
BP	1920	0	F4	0	2320
ADEG1	1920	240	G4	0	2080
C1	1920	460	B3	0	1860
E2	1920	660	A3	0	1660
D2	1920	860	F3	0	1460
C2	1920	1060	G3	0	1260
E3	1920	1260	P1, P2	0	1060
D3	1920	1460	P3, P4	0	860
C3	1920	1660	B2	0	660
E4	1920	1860	A2	0	460
D4	1920	2080	F2	0	240
C4	1920	2320	G2	0	0
B4	1680	2320	B1	240	0
S2	1460	2320	TR	460	0
S4	1260	2320	TS	660	0
V_{SS}	1060	2320	V_{DD}	860	0
Chip corner max. value	−160	−160			

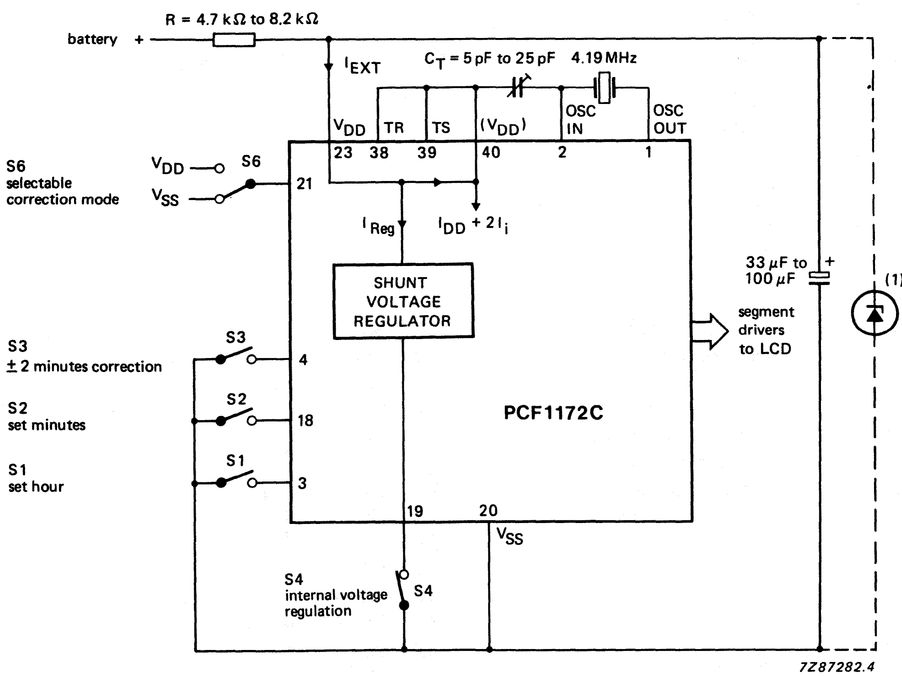
3½-DIGIT LCD CAR CLOCK CIRCUIT

GENERAL DESCRIPTION

The PCF1172C is a single chip, 4.19 MHz CMOS clock circuit indicating hours and minutes. It is designed to drive a 3½-digit liquid crystal display (LCD) with AM and PM indicators. Two single-pole, single-throw switches accomplish all time setting functions. The circuit is battery operated via an internal 5 V voltage regulator or by an external stabilized voltage supply.

Features

- Driving standard 3½-digit LCD with AM and PM indicators
- Internal voltage regulator for 5 V LCD
- Option for external stabilized voltage supply
- 4,19 MHz oscillator
- Integrated oscillator output capacitor and polarization resistor
- Operating ambient temperature range –40 to +85 °C
- 40-lead plastic-mini pack (VSO40)



(1) Only needed if internal regulation is disconnected.

Fig. 1 Typical application diagram.

Note: from pin 2 (OSC IN) to any other pin, the stray capacitance should not exceed 2 pF.

PACKAGE OUTLINES

PCF1172CT: 40-lead mini-pack; plastic (opposite bent leads) (VSO40; SOT158B).
PCF1172CU: uncased chip in tray.

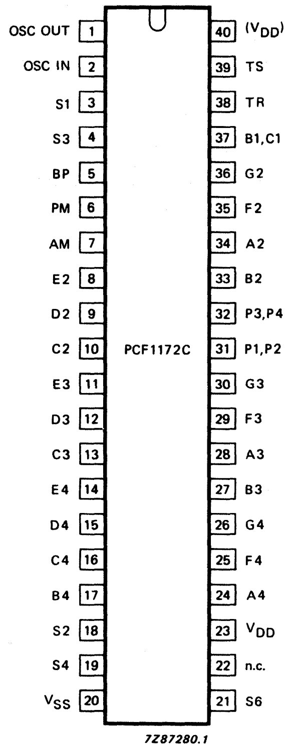


Fig. 2 Pinning diagram.

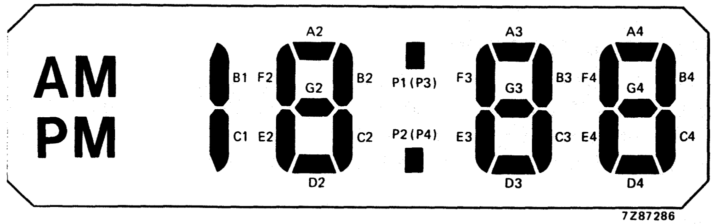


Fig. 3 Segment designation of LCD.

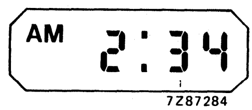
TIME


Fig. 4 12-hour display mode.

PINNING

1	OSC OUT	oscillator output
2	OSC IN	oscillator input
3	S1	set hour
4	S3	± 2 minute correction
5	BP	64 Hz backplane driver (common of LCD)
6	PM	segment outputs for PM/AM annunciators
7	AM	
8	E2	segment drivers
9	D2	
10	C2	
11	E3	
12	D3	
13	C3	
14	E4	
15	D4	
16	C4	
17	B4	
18	S2	set minutes
19	S4	internal voltage regulation
20	V_{SS}	negative supply
21	S6	selectable correction mode
22	n.c.	not connected
23	V_{DD}	positive supply
24	A4	segment drivers
25	F4	
26	G4	
27	B3	
28	A3	
29	F3	
30	G3	
31	P1, P2	colon flashing
32	P3, P4	colon static
33	B2	segment drivers
34	A2	
35	F2	
36	G2	
37	B1, C1	
38	TR	test reset; connect to (V_{DD})
39	TS	test speed-up; connect to (V_{DD})
40	(V_{DD})	positive supply for test and oscillator inputs

SWITCH FUNCTIONS

Time set mode

Switch inputs S1, S2 and S3 have an internal pull-up resistor to facilitate use of single-pole, single-throw contacts. A specific debounce circuit is integrated as protection against contact debounce and parasitic voltages.

Switch S1

Set hours, S6 selects mode of correction.

Switch S2

Set minutes, S6 selects mode of correction. When S2 is closed, in addition to the minute correction, the second counter is set to zero. Release of S2 sets the second counter running.

Switches S1 and S2

Segment test: If S1 and S2 are pressed simultaneously all LCD segments are switched on. When the switches are released, the clock starts at 1 : 00.

Switch options

Switch S3

Time correction ± 2 minutes, only operates between 58 minutes 00 seconds and 1 minute 59 seconds. By pressing S3 the clock resets to the full hour with minutes and seconds at zero.

Switch S4

Internal regulation: S4 is closed; the internal voltage regulator is active and the voltage supply for the LCD is 5 V.
External regulation: S4 is open; the circuit has to be supplied with an externally regulated voltage.

Switch S6

Single set correction mode: S6 is connected to V_{DD}; each closure of S1 or S2 advances the counter by one.
Continuous set correction mode: S6 is connected to V_{SS}; each closure of S1 or S2 advances the counter by one and after one second continues with one advance per second until S1 or S2 is released.

Testing

In normal operation the test inputs TR (pin 38) and TS (pin 39) have to be connected to V_{DD} (pin 23). A test frequency (64 Hz) is available at BP (pin 5). The test mode is activated by connecting TS to V_{SS} (pin 20). All output frequencies are then increased by a factor of 65536. In this mode the maximum input frequency is 100 kHz (external generator at OSC_{IN}). By connecting TR to V_{SS} all counters (seconds, minutes and hours) are stopped. After connecting TR to V_{DD} all counters start from an initial state.
Switch functions also operate in the test mode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage with respect to V_{SS}			
with internal regulation disconnected*	V_{DD}	max.	8 V
Voltage range (any pin)	$V_{n\text{-}20}$	V_{SS}	−0.3 to V_{DD} + 0.3 V
Storage temperature range	T_{stg}		−55 to +125 °C
Operating ambient temperature range	T_{amb}		−40 to +85 °C

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; crystal: f = 4.194304 MHz, R_s = 50 Ω, C_L = 12 pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (external regulation)	V_{DD}	3	–	6	V
Supply voltage (internal regulation I_{REG} = 1 mA)	V_{DD}	4	5	6	V
Regulation current (with internal regulation)	I_{REG}	0.2	–	5	mA
Current consumption all switches open; without LCD; internal regulation disconnected; note 1	I_{DD}	50	400	700	μA
Differential internal impedance at I_{REG} = 1 mA	r_o	–	–	150	Ω
Oscillator (pins 1 and 2); note 2					
start time	t_{osc}	–	–	200	ms
frequency stability at ΔV_{DD} = 100 mV	$\Delta f/f_{osc}$	–	0.2×10^{-6}	1×10^{-6}	
feedback resistance	R_{fb}	0.1	–	1	MΩ
input capacitance	C_i	–	–	9	pF
output capacitance	C_o	19	24	29	pF
Switches S1, S2 and S3 (pins 18, 3 and 4)					
input current with inputs connected to V_{SS}	I_i	50	150	500	μA
debounce time	t_d	32	–	150	ms
Segment driver output resistance at ± I_L = 50 μA	R_S	–	1	2.5	kΩ
Backplane driver output resistance at ± I_L = 250 μA	R_{BP}	–	0,2	0.5	kΩ
Backplane driver output frequency	f_{BP}	–	64	–	Hz
LCD d.c. offset voltage at R_L = 200 kΩ; C_L = 1 nF		–	–	±50	mV

Notes to characteristics

1. The current $I_{EXT} = I_{REG} + I_{DD} + 2 \times I_i$.
2. For correct operation of the oscillator: $V_{DD} \geqslant 3$ V.

* Connecting the supply voltage with reverse polarity, will not harm the circuit, provided the current is limited to 10 mA by the external resistor.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS

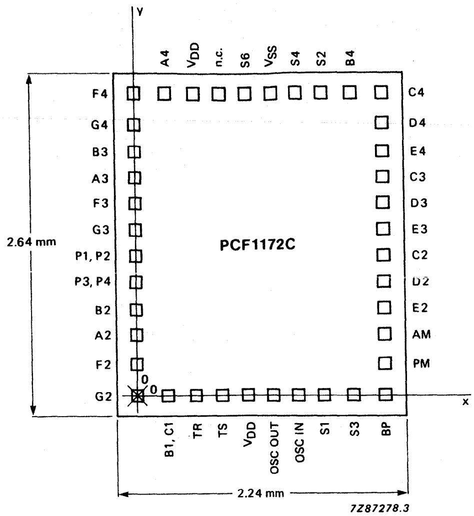


Fig. 5 Bonding pad locations; 40 terminals.

n.c.: not connected
Bonding pad dimensions 110 μm x 110 μm
Chip area = 5.91 mm^2

Table 1 Bonding pad locations (dimensions in μm)

All x/y co-ordinates are referenced to the pad G2, see Fig. 5.

pad	x	y	pad	x	y
OSC OUT	1060	0	S6	860	2320
OSC IN	1260	0	n.c.	660	2320
S1	1460	0	V_{DD}	460	2320
S3	1680	0	A4	240	2320
BP	1920	0	F4	0	2320
PM	1920	240	G4	0	2080
AM	1920	460	B3	0	1860
E2	1920	660	A3	0	1660
D2	1920	860	F3	0	1460
C2	1920	1060	G3	0	1260
E3	1920	1260	P1, P2	0	1060
D3	1920	1460	P3, P4	0	860
C3	1920	1660	B2	0	660
E4	1920	1860	A2	0	460
D4	1920	2080	F2	0	240
C4	1920	2320	G2	0	0
B4	1680	2320	B1, C1	240	0
S2	1460	2320	TR	460	0
S4	1260	2320	TS	660	0
V_{SS}	1060	2320	V_{DD}	860	0
Chip corner max. value	−160	−160			

4-DIGIT STATIC-LCD CAR CLOCK CIRCUIT

GENERAL DESCRIPTION

The PCF1174C is a single chip, 4.19 MHz CMOS car clock circuit providing hours, minutes and seconds functions. It is designed to drive a 4-digit static liquid crystal display (LCD). Two single-pole, single-throw switches accomplish all time setting functions. The frequency and voltage regulator are electrically programmable via an on-chip EEPROM. The circuit is battery operated via the internal voltage regulator and an external resistor.

Features

- Internal voltage regulator is electrically programmable for various LCD voltages
- Frequency is electrically programmable (no trimming capacitor required)
- LCD voltage adjusts with temperature for good contrast
- 4.19 MHz oscillator
- 12 hour or 24 hour mode
- Operating ambient temperature range −40 to + 85 °C
- 40-lead plastic mini-pack (VSO40)

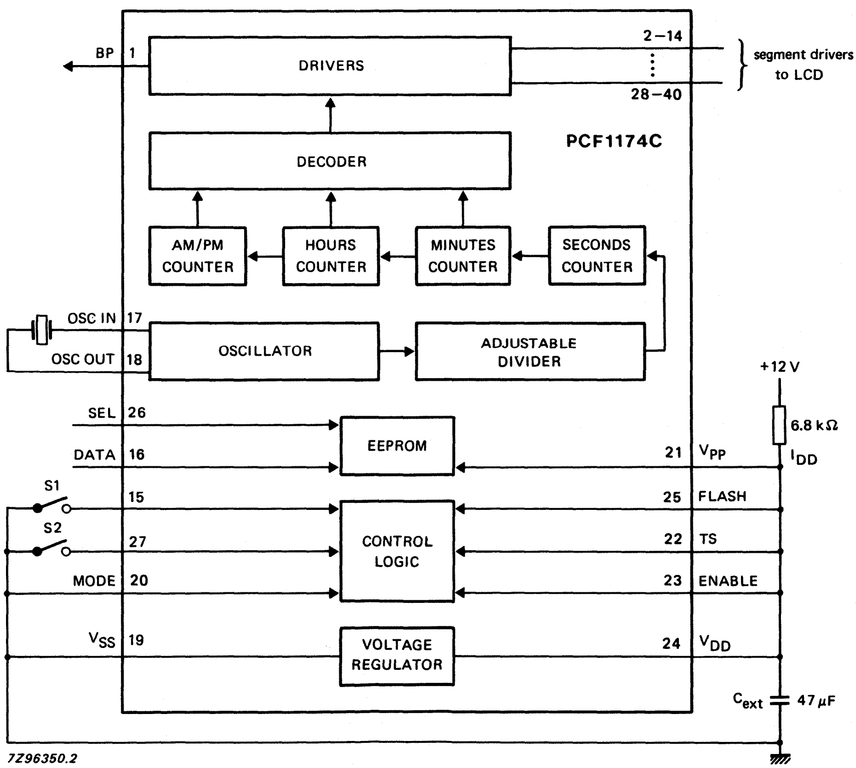


Fig.1 Typical application diagram.

PACKAGE OUTLINES

PCF1174CT: 40-lead mini-pack; plastic (opposite bent leads) (VSO40; SOT158B).
PCF1174CU: uncased chip in tray.

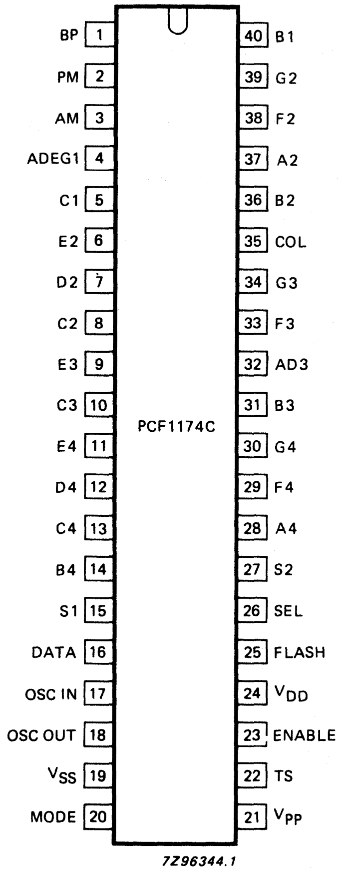


Fig.2 Pinning diagram.

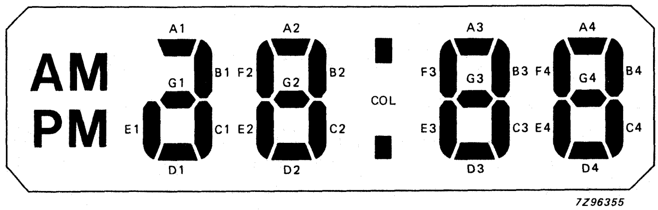
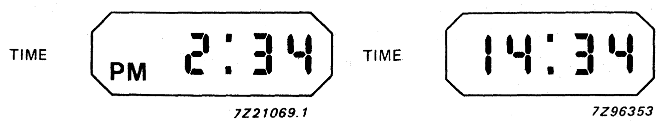


Fig.3 Segment designation of LCD.



12-hour mode

24-hour mode

Fig.4 Typical displays.

PINNING

1	BP	backplane output	21	V_{PP}	programming voltage input
2	PM		22	TS	test speed-up mode input
3	AM		23	ENABLE	set enable input for S1 and S2
4	ADEG1		24	V_{DD}	positive supply voltage
5	C1		25	FLASH	colon option input
6	E2		26	SEL	EEPROM select input
7	D2		27	S2	minute adjustment input
8	C2	segment drivers (pins 2 to 14)	28	A4	
9	E3		29	F4	
10	C3		30	G4	
11	E4		31	B3	
12	D4		32	AD3	
13	C4		33	F3	
14	B4		34	G3	segment drivers (pins 28 to 40)
15	S1	hour adjustment input	35	COL	
16	DATA	EEPROM data input	36	B2	
17	OSC IN	oscillator input	37	A2	
18	OSC OUT	oscillator output	38	F2	
19	V_{SS}	negative supply voltage	39	G2	
20	MODE	12/24 hour mode select input	40	B1	

FUNCTIONAL DESCRIPTION AND TESTING

Outputs

The circuit outputs static data to the LCD. Generation of BP and the output signals are shown in Fig.5.

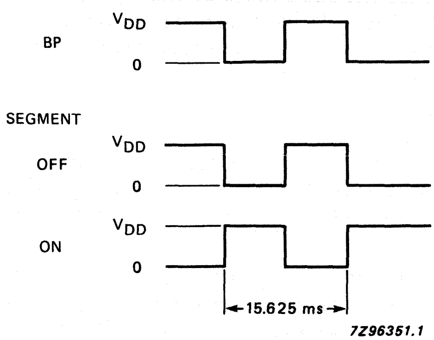


Fig.5 Backplane and output signals.

The average voltages across the segments are:

$V_{ON(rms)} = V_{DD}$
$V_{OFF(rms)} = 0$ V.

LCD voltage

The adjustable voltage regulator controls the supply voltage (see section 'LCD voltage programming') in relation to temperature for good contrast e.g. when V_{DD} = 4.5 V at + 25 °C, then:

V_{DD} = 3 to 4 V at + 85 °C
V_{DD} = 5 to 6 V at −40 °C.

12/24-hour mode

Operation in 12-hour or 24-hour mode is selected by connecting MODE to V_{DD} or V_{SS} respectively.

Power-on

After connecting the supply, the start-up mode is:

1:00 AM; 12-hour mode
0:00 ; 24-hour mode.

Colon

If FLASH is connected to V_{DD}, the colon pulses at 1 Hz. If FLASH is connected to V_{SS}, the colon is static.

Time setting

Switches S1 and S2 have a pull-up resistor to facilitate the use of single-pole, single-throw contacts. A debounce circuit is incorporated to protect against contact bounce and parasitic voltages.

Set enable

Inputs S1 and S2 are enabled by connecting ENABLE to V_{DD} or disabled by connecting to V_{SS}.

Set hours

When S1 is connected to V_{SS} the hours displayed advances by one and then continues with one advance per second until S1 is released (auto-increment).

Set minutes

When S2 is connected to V_{SS} the time displayed in minutes advances by one and after one second continues with one advance per second until S2 is released (auto-increment). In addition to minute correction, the seconds counter is reset to zero.

Segment test/reset

When S1 and S2 are connected to V_{SS}, all LCD segments are switched ON. Releasing S1 and S2 resets the display. No reset occurs when DATA is connected to V_{SS} (overlapping S1 and S2).

Test mode

When TS is connected to V_{DD}, the device is in normal operating mode. When connecting TS to V_{SS} all counters (seconds, minutes and hours) are stopped, allowing quick testing of the display via S1 and S2 (debounce and auto-increment times are 64 times faster). TS has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

EEPROM

V_{PP} has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

LCD voltage programming

To enable LCD voltage programming, SEL is set to open-circuit and a level of V_{DD} −5 V is applied to V_{PP} (see Fig.7). The first pulse (t_E) applied to the DATA input clears the EEPROM to give the lowest voltage output. Further pulses (t_L) will increment the output voltage by steps of typically 150 mV (T_{amb} = 25 °C). For programming, measure $V_{DD} - V_{SS}$ and apply a store pulse (t_W) when the required value is reached. If the maximum number of steps (n = 31) is reached and an additional pulse is applied the voltage will return to the lowest value.

Frequency

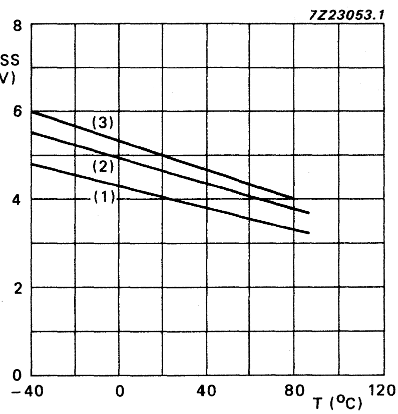
Electronic adjustment of the frequency eliminates the requirement for an external trimming capacitor. The quartz frequency has been positively offset (nominal deviation + 60×10^{-6}) by capacitors at the oscillator input and output.

Frequency programming

To enable frequency programming, SEL is set to V_{SS} and a level of V_{DD} −5 V is applied to V_{PP} (see Fig.7). The first pulse (t_E) applied to the DATA input clears the EEPROM to give the highest frequency. Additional pulses (t_L) decrement the frequency in steps as shown in Table 1. Measurement of the backplane period provides a method of checking the new frequency to be programmed. Once the required frequency is obtained, apply a store pulse (t_W) and release SEL. If the minimum frequency is reached and an additional pulse is applied the frequency will return to the highest programmable value.

Table 1 Frequency programming ($\Delta t = 3.81\ \mu s$)

frequency deviation $\Delta f/f$ (ppm)	number of pulses n	backplane period (ms)
−3.8	1	15.629
−7.6	2	15.633
−11.4	3	15.636
.	.	.
.	.	.
.	.	.
−117.8	31	15.743



(1) programmed to 4.0 V at 25 °C
(2) programmed to 4.5 V at 25 °C
(3) programmed to 5.0 V at 25 °C
values within the specified operating range.

Fig.6 Regulated voltage as a function of temperature (typical).

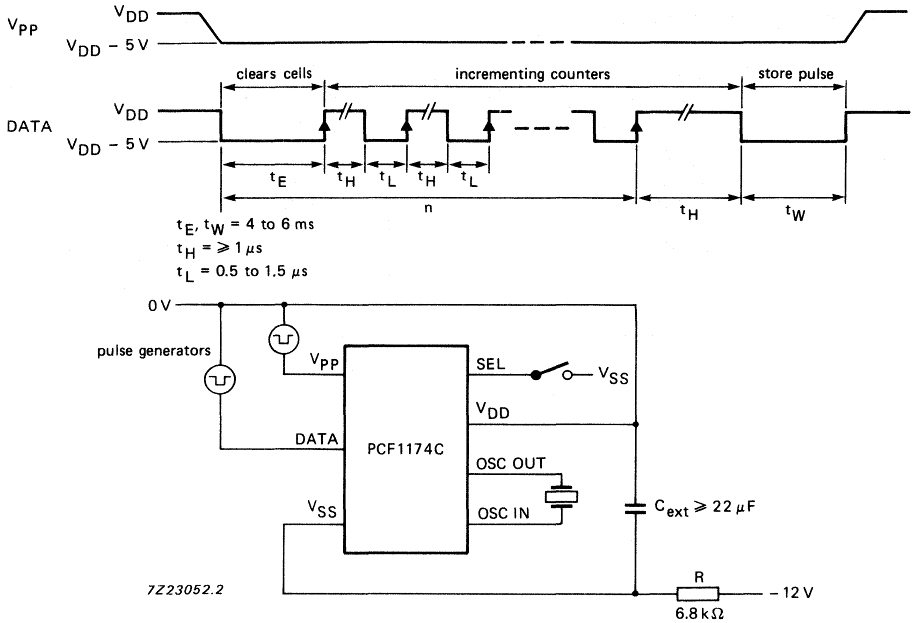


Fig.7 Programming diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	w.r.t V_{SS}	V_{DD}	–	8	V
Supply current	V_{SS} = 0 V; note 1	I_{DD}	–	3	mA
Voltage range	all pins except V_{PP} and DATA	V_I	−0.3	V_{DD} + 0.3	V
Voltage range	pins V_{PP} and DATA	V_I	−3.0	V_{DD} + 0.3	V
Storage temperature range		T_{stg}	−55	+ 125	°C
Operating ambient temperature range		T_{amb}	−40	+ 85	°C

Note to the ratings

1. Connecting the supply voltage with reverse polarity, will not harm the circuit, provided the current is limited to 10 mA by an external resistor.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

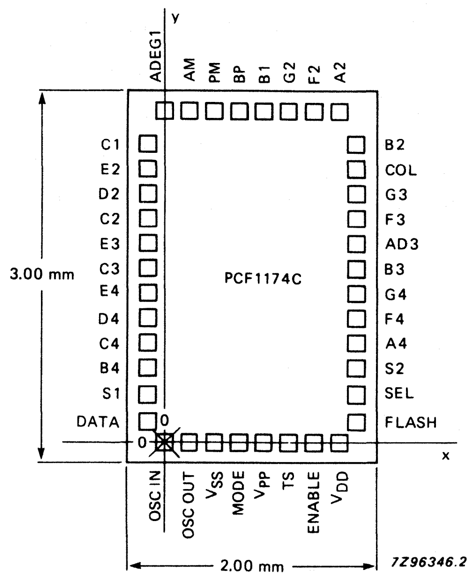
V_{DD} = 3 to 6 V; V_{SS} = 0 V; T_{amb} = –40 to + 85 °C; crystal: frequency = 4.194304 MHz; R_S = 50 Ω, C_L = 12 pF; maximum frequency tolerance = ± 30 x 10^{-6}; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	voltage regulator programmed to 4.5 V at T_{amb} = 25 °C	V_{DD}	3	–	6	V
Supply voltage variation	S1 or S2 closed	ΔV_{DD}	–	–	50	mV
Supply voltage variation due to temperature		TC	–	–0.35	–	%/K
	V_{DD} = 4.5 V	TC	–	–16	–	mV/K
Supply current	note 1	I_{DD}	900	1500	2000	μA
Capacitance	external capacitor	C_{EXT}	22	47	–	μF
Oscillator						
Start time		t_{OSC}	–	–	200	ms
Frequency deviation	nominal n = 0	Δf/f	0	+ 60x10^{-6}	+ 120x10^{-6}	
Frequency stability	ΔV_{DD} = 100 mV	Δf/f	–	–	1x10^{-6}	
Input capacitance		C_I	–	16	–	pF
Output capacitance		C_O	–	27	–	pF
Feedback resistance		R_{fb}	300	1000	3000	kΩ
Inputs						
Pull-up resistance	S1, S2, TS, SEL and DATA	R_O	45	90	180	kΩ
Leakage current	FLASH, ENABLE, MODE	I_{IL}	–	–	2	μA
Debounce time	S1 and S2 only	t_d	30	65	100	ms
V_{PP} programming voltage						
Output current	V_{PP} = V_{DD} – 5 V	I_{O2}	70	–	700	μA
Output current	during programming	I_{O2}	–	500	–	μA
Backplane	high and low levels					
Output resistance	± 100 μA	R_{BP}	–	–	3	kΩ
Segment						
Output resistance	± 100 μA	R_{SEG}	–	–	5	kΩ
LCD						
DC offset voltage	200 kΩ/1 nF	V_{DC}	–	–	50	mV

Notes to the characteristics

1. A suitable resistor (R) must be selected:
   Example: V_{DD} = 5 V, R max. (12 V – 5 V)/ 900 μA = 7.8 kΩ
   V_{DD} = 5 V, R typ. (12 V – 5 V)/1500 μA = 4.7 kΩ (more reserve).

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 6 mm^2
Bonding pad dimensions: 100 μm x 100 μm

Fig.8 Bonding pad locations.

Table 3 Bonding pad locations (dimensions in μm)
All x/y co-ordinates are referenced to the bottom left pad (OSC IN), see Fig.8.

pad	X	Y	pad	X	Y
BP	600	2676	V_{PP}	800	0
PM	400	2676	TS	1000	0
AM	200	2676	ENABLE	1200	0
ADEG1	0	2676	V_{DD}	1400	0
C1	−138	2448	FLASH	1538	168
E2	−138	2228	SEL	1538	388
D2	−138	2008	S2	1538	608
C2	−138	1808	A4	1538	808
E3	−138	1608	F4	1538	1008
C3	−138	1408	G4	1538	1208
E4	−138	1208	B3	1538	1408
D4	−138	1008	AD3	1538	1608
C4	−138	808	F3	1538	1808
B4	−138	608	G3	1538	2008
S1	−138	388	COL	1538	2208
DATA	−138	168	B2	1538	2448
OSC IN	0	0	A2	1400	2676
OSC OUT	200	0	F2	1200	2676
V_{SS}	400	0	G2	1000	2676
MODE	600	0	B1	800	2676
chip corner (max.)	−300	−160			

4-DIGIT DUPLEX-LCD CAR CLOCK CIRCUIT

GENERAL DESCRIPTION

The PCF1175C is a single chip, 4.19 MHz CMOS car clock circuit providing hours, minutes and seconds functions. It is designed to drive a 4-digit duplex liquid crystal display (LCD). Two single-pole, single-throw switches accomplish all time setting functions. The frequency and voltage regulator are electrically programmable via an on-chip EEPROM. The circuit is battery operated via the internal voltage regulator and an external resistor.

Features

- Internal voltage regulator is electrically programmable for various LCD voltages
- Frequency is electrically programmable (no trimming capacitor required)
- LCD voltage adjusts with temperature for good contrast
- 4.19 MHz oscillator
- 12 hour or 24 hour mode
- Operating ambient temperature range −40 to + 85 °C
- 28-lead plastic mini-pack

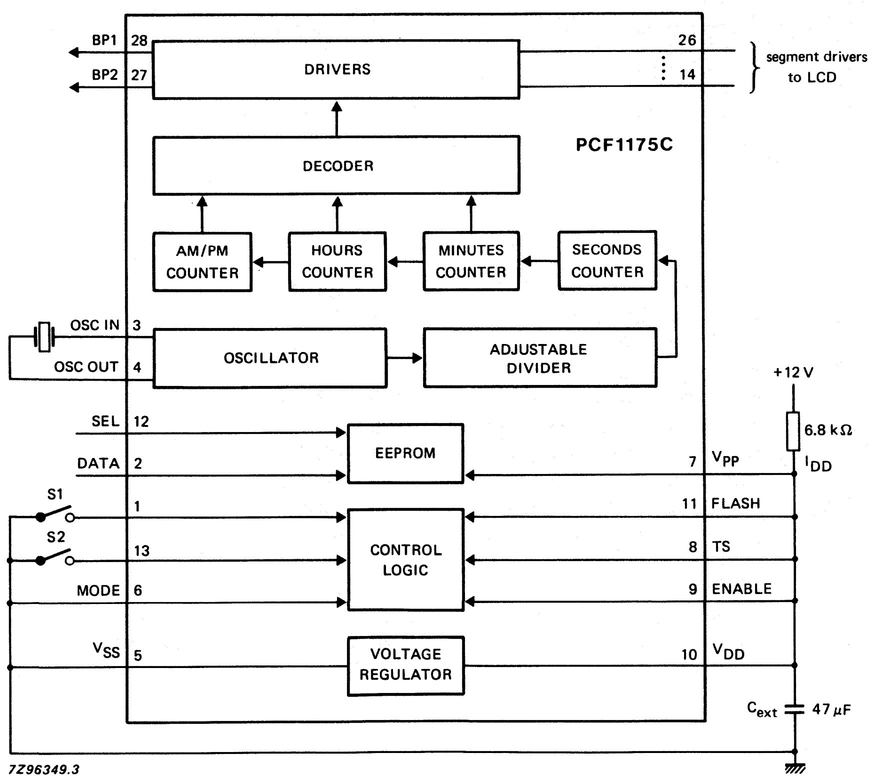


Fig.1 Typical application diagram.

PACKAGE OUTLINES

PCF1175CT: 28-lead mini-pack; plastic (SO28; SOT136A).
PCF1175CU: uncased chip in tray.
PCF1175CU/10: chip-on-film frame carrier (FFC).

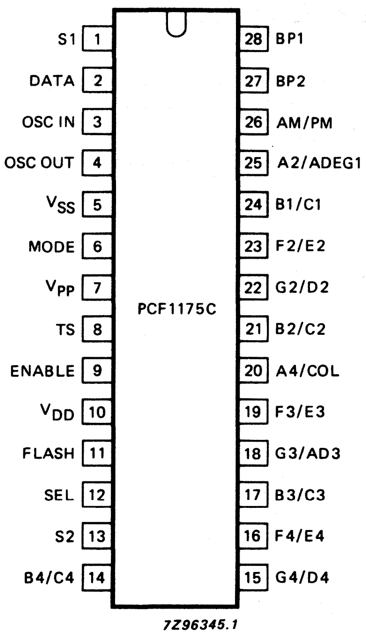


Fig.2 Pinning diagram.

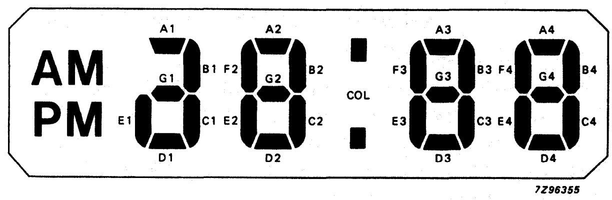
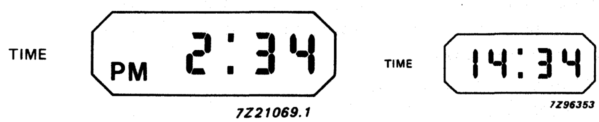


Fig.3 Segment designation of LCD.



12-hour mode

24-hour mode

Fig.4 Typical displays.

PINNING

1	S1	hour adjustment input	15	G4/D4	segment drivers
2	DATA	EEPROM data input	16	F4/E4	
3	OSC IN	oscillator input	17	B3/C3	
4	OSC OUT	oscillator output	18	G3/AD3	
5	V_{SS}	negative supply voltage	19	F3/E3	
6	MODE	12/24 hour mode select input	20	A4/COL	
7	V_{PP}	programming voltage input	21	B2/C2	
8	TS	test speed-up mode input	22	G2/D2	
9	ENABLE	enable input (for S1 and S2)	23	F2/E2	
10	V_{DD}	positive supply voltage	24	B1/C1	
11	FLASH	colon option input	25	A2/ADEG1	
12	SEL	EEPROM select input	26	AM/PM	
13	S2	minute adjustment input	27	BP2	backplane 2
14	B4/C4	segment drivers	28	BP1	backplane 1

FUNCTIONAL DESCRIPTION AND TESTING

Outputs

The circuit outputs 1:2 multiplexed data (duplex) to the LCD. Generation of BP1 and BP2 (three-level backplane signals) and the output signals are shown in Fig.5.

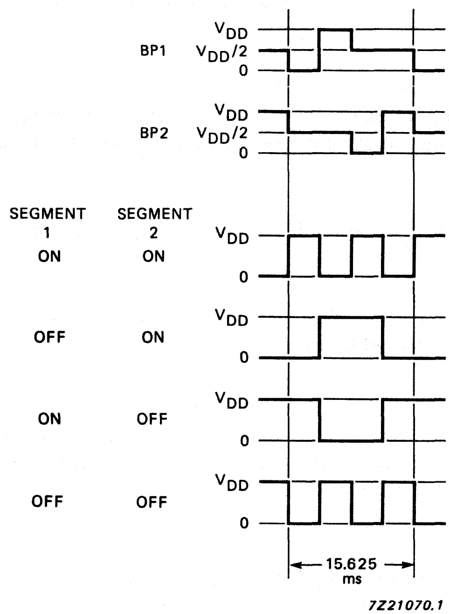


Fig.5 Backplane and output signals.

The average voltages across the segments are:

$V_{ON(rms)} = 0.79\ V_{DD}$
$V_{OFF(rms)} = 0.35\ V_{DD}$

LCD voltage

The adjustable voltage regulator controls the supply voltage (see section 'LCD voltage programming') in relation to temperature for good contrast e.g. when $V_{DD} = 4.5$ V at 25 °C, then:

$V_{DD} = 3$ to 4 V at +85 °C
$V_{DD} = 5$ to 6 V at −40 °C.

12/24-hour mode

Operation in 12-hour or 24-hour mode is selected by connecting MODE to V_{DD} or V_{SS} respectively. If MODE is left open-circuit and a reset occurs, the mode will change from 12-hour to 24-hour mode or vice versa.

Power-on

After connecting the supply, the start-up mode is:

1:00 AM; 12-hour mode (MODE connected to V_{DD})
0:00 ; 24-hour mode (MODE connected to V_{SS} or left open-circuit).

Colon

If FLASH is connected to V_{DD}, the colon pulses at 1 Hz. If FLASH is connected to V_{SS}, the colon is static.

Time setting

Switches S1 and S2 have a pull-up resistor to facilitate the use of single-pole, single-throw contacts. A debounce circuit is incorporated to protect against contact bounce and parasitic voltages.

Set enable

Inputs S1 and S2 are enabled by connecting ENABLE to V_{DD} or disabled by connecting to V_{SS}.

Set hours

When S1 is connected to V_{SS} the hours displayed advances by one and then continues with one advance per second until S1 is released (auto-increment).

Set minutes

When S2 is connected to V_{SS} the time displayed in minutes advances by one and after one second continues with one advance per second until S2 is released (auto-increment). In addition to minute correction, the seconds counter is reset to zero.

Segment test/reset

When S1 and S2 are connected to V_{SS}, all LCD segments are switched ON. Releasing S1 and S2 resets the display. No reset occurs when DATA is connected to V_{SS} (overlapping S1 and S2).

Test mode

When TS is connected to V_{DD}, the device is in normal operating mode.
When connecting TS to V_{SS} all counters (seconds, minutes and hours) are stopped, allowing quick testing of the display via S1 and S2 (debounce and auto-increment times are 64 times faster). TS has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

EEPROM

V_{PP} has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

LCD voltage programming

To enable LCD voltage programming, SEL is set to open-circuit and a level of V_{DD} −5 V is applied to V_{PP} (see Fig.7). The first pulse (t_E) applied to the DATA input clears the EEPROM to give the lowest voltage output. Additional pulses (t_L) will increment the output voltage by steps of typically 150 mV (T_{amb} = 25 °C). For programming, measure $V_{DD} - V_{SS}$ and apply a store pulse (t_W) when the required value is reached. If the maximum number of steps (n = 31) is reached and an additional pulse is applied the voltage will return to the lowest value.

Frequency

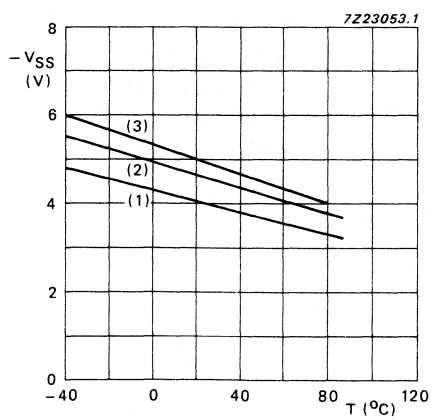
Electronic adjustment of the frequency eliminates the requirement for an external trimming capacitor. The quartz frequency has been positively offset (nominal deviation + 60 x 10^{-6}) by capacitors at the oscillator input and output.

Frequency programming

To enable frequency programming, SEL is set to V_{SS} and a level of V_{DD} −5 V is applied to V_{PP} (see Fig.7). The first pulse (t_E) applied to the DATA input clears the EEPROM to give the highest frequency. Additional pulses (t_L) decrement the frequency in steps as shown in Table 1. Measurement of the backplane period provides a method of checking the new frequency to be programmed. Once the required frequency is obtained, apply a store pulse (t_W) and release SEL. If the minimum frequency is reached and an additional pulse is applied the frequency will return to the highest programmable value.

Table 1 Frequency programming (Δt = 7.63 μs)

frequency deviation $\Delta f/f$ (ppm)	number of pulses n	backplane period (ms)
−3.8	1	15.633
−7.6	2	15.641
−11.4	3	15.648
.	.	.
.	.	.
−117.8	31	15.861



(1) programmed to 4.0 V at 25 °C
(2) programmed to 4.5 V at 25 °C   values within the specified operating range
(3) programmed to 5.0 V at 25 °C

Fig.6 Regulated voltage as a function of temperature (typical).

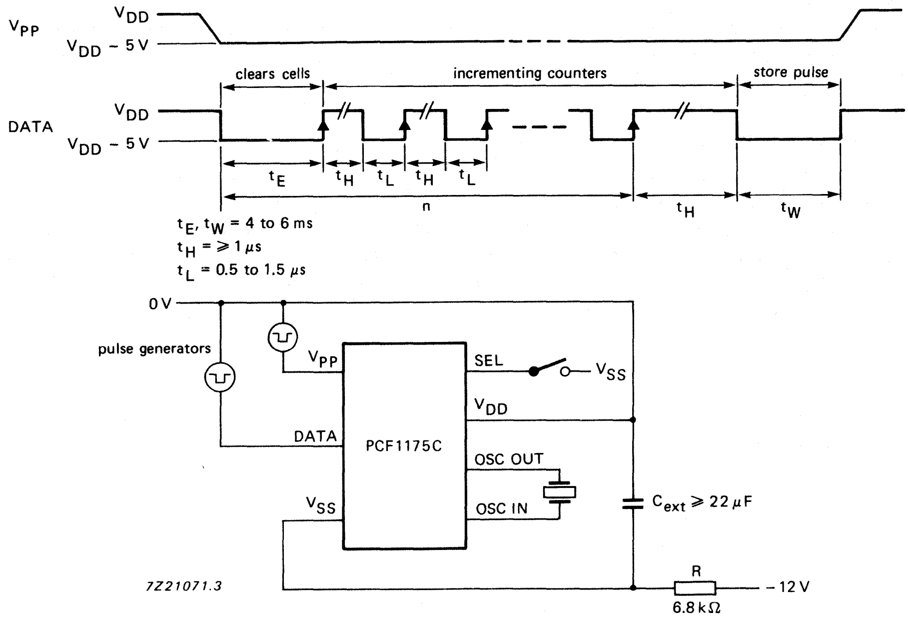


Fig.7 Programming diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	w.r.t V_{SS}	V_{DD}	–	8	V
Supply current	V_{SS} = 0 V; note 1	I_{DD}	–	3	mA
Voltage range	all pins except V_{PP} and DATA	V_I	−0.3	V_{DD} + 0.3	V
Voltage range	pins V_{PP} and DATA	V_I	−3.0	V_{DD} + 0.3	V
Storage temperature range		T_{stg}	−55	+ 125	°C
Operating ambient temperature range		T_{amb}	−40	+ 85	°C

Note to the ratings

1. Connecting the supply voltage with reverse polarity will not harm the circuit, provided the current is limited to 10 mA by an external resistor.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

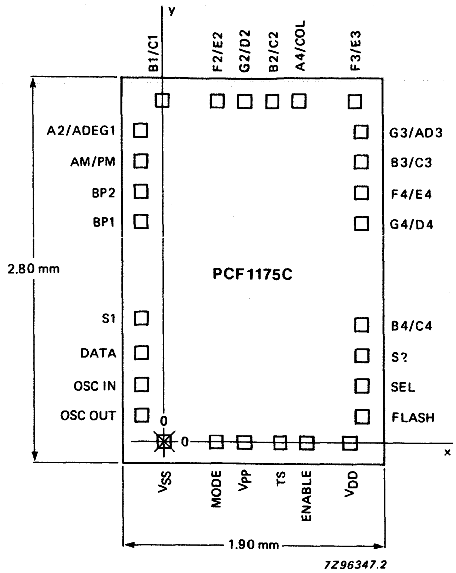
V_{DD} = 3 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; crystal: frequency = 4.194304 MHz; R_s = 50 Ω; C_L = 12 pF; maximum frequency tolerance = ± 30 x 10^{-6}; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	voltage regulator programmed to 4.5 V at T_{amb} = 25 °C	V_{DD}	3	–	6	V
Supply voltage variation	S1 or S2 closed	ΔV_{DD}	–	–	50	mV
Supply voltage variation due to temperature		TC	–	−0.35	–	%/K
	V_{DD} = 4.5 V	TC	–	−16	–	mV/K
Supply current	note 1	I_{DD}	900	1500	2000	μA
Capacitance	external capacitor	C_{EXT}	22	47	–	μF
Oscillator						
Start time		t_{OSC}	–	–	200	ms
Frequency deviation	nominal n = 0	$\Delta f/f$	0	+ 60x10^{-6}	+ 120x10^{-6}	
Frequency stability	ΔV_{DD} = 100 mV	$\Delta f/f$	–	–	1x10^{-6}	
Input capacitance		C_I	–	16	–	pF
Output capacitance		C_O	–	27	–	pF
Feedback resistance		R_{fb}	300	1000	3000	kΩ
Inputs						
Pull-up resistance	S1, S2, TS, SEL and DATA	R_O	45	90	180	kΩ
Leakage current	ENABLE, FLASH	I_{IL}	–	–	2	μA
Pull-up/pull-down resistance	MODE	R_O	100	300	1000	kΩ
Debounce time	S1 and S2 only	t_d	30	65	100	ms
V_{PP} programming voltage						
Output current	V_{PP} = V_{DD} − 5 V	I_{O2}	70	–	700	μA
Output current	during programming	I_{O2}	–	500	–	μA
Backplane	high and low levels					
Output resistance	± 100 μA	R_{BP}	–	–	3	kΩ
Segment						
Output resistance	± 100 μA	R_{SEG}	–	–	5	kΩ
LCD						
DC offset voltage	200 kΩ/1 nF	V_{DC}	–	–	50	mV

Notes to characteristics

1. A suitable external resistor (R) must be selected:
   Example: V_{DD} = 5 V, R max. (12 V − 5 V)/ 900 μA = 7.8 kΩ
   V_{DD} = 5 V, R typ. (12 V − 5 V)/ 1500 μA = 4.7 kΩ (more reserve).

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 5.32 mm^2
Bonding pad dimensions: 100 μm x 100 μm

Fig.8 Bonding pad locations.

Table 3 Bonding pad locations (dimensions in μm)
All x/y co-ordinates are referenced to the bottom left pad (V_{SS}), see Fig.8.

pad	X	Y	pad	X	Y
S1	−138	881	G4/D4	1438	1588
DATA	−138	639	F4/E4	1438	1808
OSC IN	−138	408	B3/C3	1438	2028
OSC OUT	−138	188	G3/AD3	1438	2248
V_{SS}	0	0	F3/E3	1400	2476
MODE	383	0	A4/COL	1000	2476
V_{PP}	583	0	B2/C2	800	2476
TS	846	0	G2/D2	600	2476
ENABLE	1046	0	F2/E2	400	2476
V_{DD}	1352	0	B1/C1	0	2476
FLASH	1438	188	A2/ADEG1	−138	2248
SEL	1438	408	AM/PM	−138	2028
S2	1438	628	BP2	−138	1808
B4/C4	1438	848	BP1	−138	1588
chip corner (max.)	−300	−160			

4-DIGIT DUPLEX-LCD CAR CLOCK CIRCUIT

GENERAL DESCRIPTION

The PCF1178C is a single chip, 4.19 MHz CMOS car clock circuit providing hours, minutes and seconds functions. It is designed to drive a 4-digit duplex liquid crystal display (LCD). Two single-pole, single-throw switches accomplish all time setting functions. The frequency and voltage regulator are electrically programmable via an on-chip EEPROM. The circuit is battery operated via the internal voltage regulator and an external resistor.

Features

- Internal voltage regulator is electrically programmable for various LCD voltages
- Frequency is electrically programmable (no trimming capacitor required)
- LCD voltage adjusts with temperature for good contrast
- 4.19 MHz oscillator
- 12 hour or 24 hour mode
- Operating ambient temperature range –40 to + 85 °C

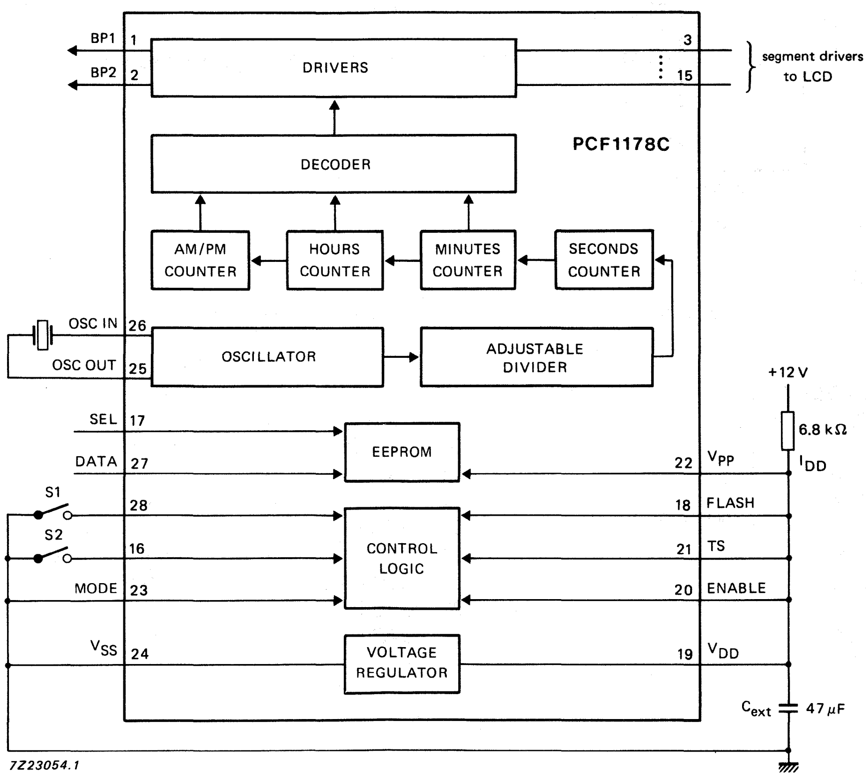


Fig.1 Typical application diagram.

PACKAGE OUTLINES

PCF1178CT:	28-lead mini-pack; plastic (SO28; SOT136A).
PCF1178CU:	uncased chip in tray.
PCF1178CU/10:	chip-on-film frame carrier (FFC).
PCF1178CU/5:	unsawn wafer.

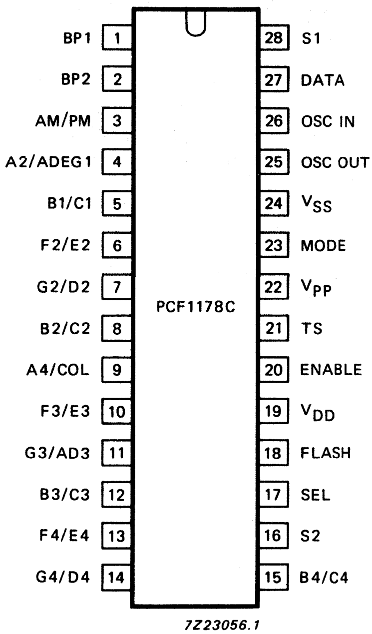


Fig.2 Pinning diagram.

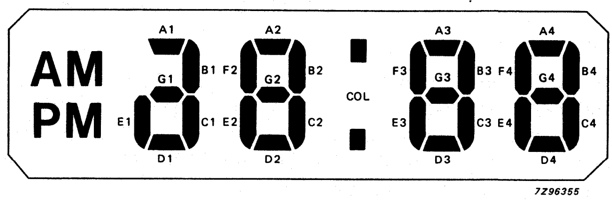
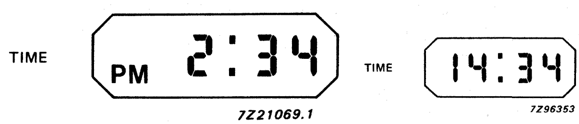


Fig.3 Segment designation of LCD.



12-hour mode 24-hour mode

Fig.4 Typical displays.

PINNING

1	BP1	backplane 1	15	B4/C4	segment drivers
2	BP2	backplane 2	16	S2	minute adjustment input
3	AM/PM	segment drivers	17	SEL	EEPROM select input
4	A2/ADEG1	segment drivers	18	FLASH	colon option input
5	B1/C1	segment drivers	19	V_{DD}	positive supply voltage
6	F2/E2	segment drivers	20	ENABLE	enable input (for S1 and S2)
7	G2/D2	segment drivers	21	TS	test speed-up mode input
8	B2/C2	segment drivers	22	V_{PP}	programming voltage input
9	A4/COL	segment drivers	23	MODE	12/24 hour mode select input
10	F3/E3	segment drivers	24	V_{SS}	negative supply voltage
11	G3/AD3	segment drivers	25	OSC OUT	oscillator output
12	B3/C3	segment drivers	26	OSC IN	oscillator input
13	F4/E4	segment drivers	27	DATA	EEPROM data input
14	G4/D4	segment drivers	28	S1	hour adjustment input

FUNCTIONAL DESCRIPTION AND TESTING

Outputs

The circuit outputs 1:2 multiplexed data (duplex) to the LCD. Generation of BP1 and BP2 (three-level backplane signals) and the output signals are shown in Fig.5.

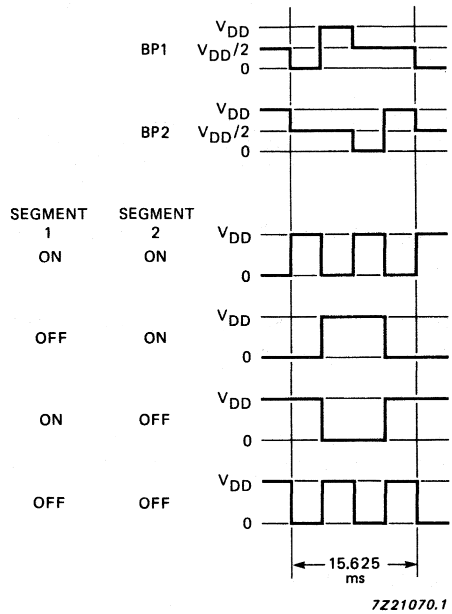


Fig.5 Backplane and output signals.

The average voltages across the segments are:

$V_{ON(rms)} = 0.79\ V_{DD}$
$V_{OFF(rms)} = 0.35\ V_{DD}$

LCD voltage

The adjustable voltage regulator controls the supply voltage (see section 'LCD voltage programming') in relation to temperature for good contrast e.g. when $V_{DD} = 4.5$ V at 25 °C, then:

$V_{DD} = 3$ to 4 V at +85 °C
$V_{DD} = 5$ to 6 V at –40 °C.

12/24-hour mode

Operation in 12-hour or 24-hour mode is selected by connecting MODE to V_{DD} or V_{SS} respectively. If MODE is left open-circuit and a reset occurs, the mode will change from 12-hour to 24-hour mode or vice versa.

Power-on

After connecting the supply, the start-up mode is:

1:00 AM; 12-hour mode (MODE connected to V_{DD})
0:00 ; 24-hour mode (MODE connected to V_{SS} or left open-circuit).

Colon

If FLASH is connected to V_{DD}, the colon pulses at 0.5 Hz. If FLASH is connected to V_{SS}, the colon is static.

Time setting

Switches S1 and S2 have a pull-up resistor to facilitate the use of single-pole, single-throw contacts. A debounce circuit is incorporated to protect against contact bounce and parasitic voltages.

Set enable

Inputs S1 and S2 are enabled by connecting ENABLE to V_{DD} or disabled by connecting to V_{SS}.

Set hours

When S1 is connected to V_{SS} the hours displayed advances by one and then continues with one advance per 0.5 s until S1 is released (auto-increment).

Set minutes

When S2 is connected to V_{SS} the time displayed in minutes advances by one and then continues with one advance per 0.5 s until S2 is released (auto-increment). In addition to minute correction, the seconds counter is reset to zero.

Segment test/reset

When S1 and S2 are connected to V_{SS}, all LCD segments are switched ON. Releasing S1 and S2 resets the display. No reset occurs when DATA is connected to V_{SS} (overlapping S1 and S2).

Test mode

When TS is connected to V_{DD}, the device is in normal operating mode. When connecting TS to V_{SS} all counters (seconds, minutes and hours) are stopped, allowing quick testing of the display via S1 and S2 (debounce and auto-increment times are 64 times faster). TS has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

EEPROM

V_{PP} has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

LCD voltage programming

To enable LCD voltage programming, SEL is set to open-circuit and a level of V_{DD} −5 V is applied to V_{PP} (see Fig.7). The first pulse (t_E) applied to the DATA input clears the EEPROM to give the lowest voltage output. Additional pulses (t_L) will increment the output voltage by steps of typically 150 mV (T_{amb} = 25 °C). For programming, measure $V_{DD} - V_{SS}$ and apply a store pulse (t_W) when the required value is reached. If the maximum number of steps (n = 31) is reached and an additional pulse is applied the voltage will return to the lowest value.

Frequency

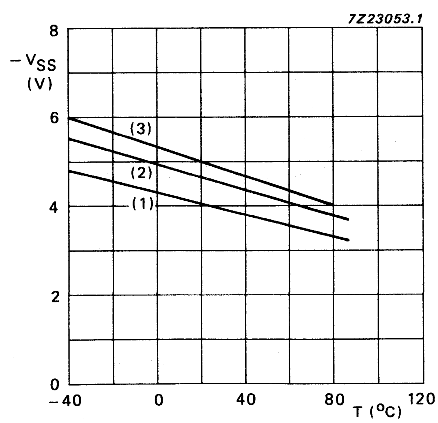
Electronic adjustment of the frequency eliminates the requirement for an external trimming capacitor. The quartz frequency has been positively offset (nominal deviation $+ 60 \times 10^{-6}$) by capacitors at the oscillator input and output.

Frequency programming

To enable frequency programming, SEL is set to V_{SS} and a level of V_{DD} −5 V is applied to V_{PP} (see Fig.7). The first pulse (t_E) applied to the DATA input clears the EEPROM to give the highest frequency. Additional pulses (t_L) decrement the frequency in steps as shown in Table 1. Measurement of the backplane period provides a method of checking the new frequency to be programmed. Once the required frequency is obtained, apply a store pulse (t_W) and release SEL. If the minimum frequency is reached and an additional pulse is applied the frequency will return to the highest programmable value.

Table 1 Frequency programming ($\Delta t = 7.63\ \mu s$)

frequency deviation Δf/f (ppm)	number of pulses n	backplane period (ms)
−3.8	1	15.633
−7.6	2	15.641
−11.4	3	15.648
.	.	.
.	.	.
−117.8	31	15.861



(1) programmed to 4.0 V at 25 °C
(2) programmed to 4.5 V at 25 °C } values within the specified operating range
(3) programmed to 5.0 V at 25 °C

Fig.6 Regulated voltage as a function of temperature (typical).

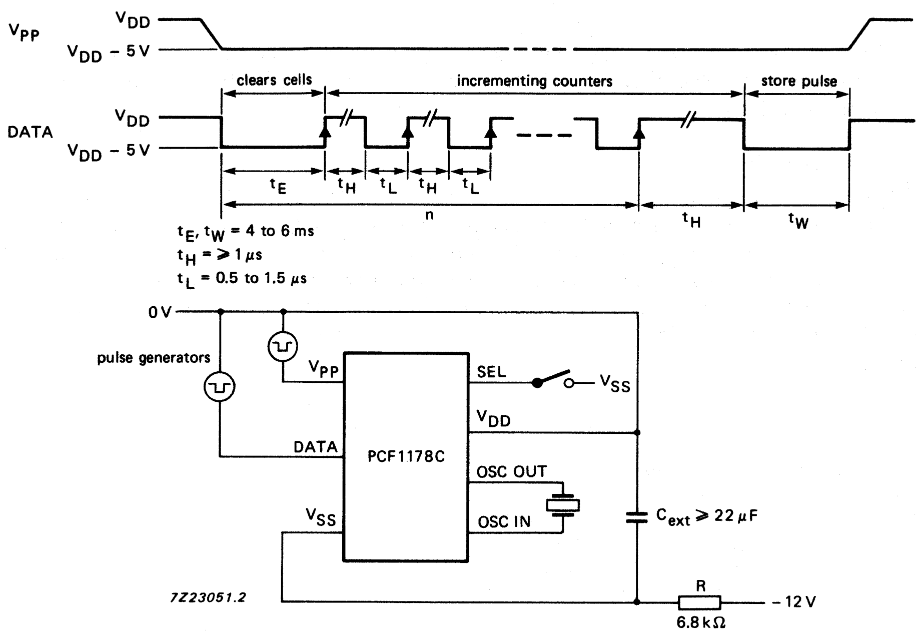


Fig.7 Programming diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	w.r.t V_{SS}	V_{DD}	–	8	V
Supply current	V_{SS} = 0 V; note 1	I_{DD}	–	3	mA
Voltage range	all pins except V_{PP} and DATA	V_I	–0.3	V_{DD} + 0.3	V
Voltage range	pins V_{PP} and DATA	V_I	–3.0	V_{DD} + 0.3	V
Storage temperature range		T_{stg}	–55	+ 125	°C
Operating ambient temperature range		T_{amb}	–40	+ 85	°C

Note to the ratings

1. Connecting the supply voltage with reverse polarity will not harm the circuit, provided the current is limited to 10 mA by an external resistor.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 3 to 6 V; V_{SS} = 0 V; T_{amb} = –40 to + 85 °C; crystal: frequency = 4.194303 MHz; R_s = 50 Ω, C_L = 12 pF; maximum frequency tolerance = ± 30 x 10^{-6}; unless otherwise specified

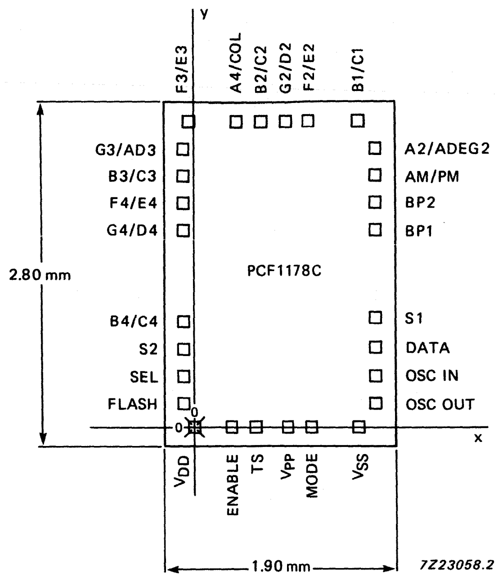
parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	voltage regulator programmed to 4.5 V at T_{amb} = 25 °C	V_{DD}	3	–	6	V
Supply voltage variation	S1 or S2 closed	ΔV_{DD}	–	–	50	mV
Supply voltage variation due to temperature		TC	–	–0.35	–	%/K
	V_{DD} = 4.5 V	TC	–	–16	–	mV/K
Supply current	note 1	I_{DD}	900	1500	2000	μA
Capacitance	external capacitor	C_{EXT}	22	47	–	μF
Oscillator						
Start time		t_{OSC}	–	–	200	ms
Frequency deviation	nominal n = 0	Δf/f	0	+ 60x10^{-6}	+ 120x10^{-6}	
Frequency stability	ΔV_{DD} = 100 mV	Δf/f	–	–	1x10^{-6}	
Input capacitance		C_I	–	16	–	pF
Output capacitance		C_O	–	27	–	pF
Feedback resistance		R_{fb}	300	1000	3000	kΩ
Inputs						
Pull-up resistance	S1, S2, TS, SEL and DATA	R_O	45	90	180	kΩ
Leakage current	ENABLE, FLASH	I_{IL}	–	–	2	μA
Pull-up/pull-down resistance	MODE	R_O	100	300	1000	kΩ
Debounce time	S1 and S2 only	t_d	30	65	100	ms
V_{PP} programming voltage						
Output current	$V_{PP} = V_{DD} - 5$ V	I_{O2}	70	–	700	μA
Output current	during programming	I_{O2}	–	500	–	μA
Backplane	high and low levels					
Output resistance	± 100 μA	R_{BP}	–	–	3	kΩ
Segment						
Output resistance	± 100 μA	R_{SEG}	–	–	5	kΩ
LCD						
DC offset voltage	200 kΩ/1 nF	V_{DC}	–	–	50	mV

Notes to characteristics

1. A suitable resistor (R) must be selected:

   Example: V_{DD} = 5 V, R max. (12 V – 5 V)/ 900 μA = 7.8 kΩ
   V_{DD} = 5 V, R typ. (12 V – 5 V)/1500 μA = 4.7 kΩ (more reserve).

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 5.32 mm^2
Bonding pad dimensions: 100 μm x 100 μm

Fig.8 Bonding pad locations.

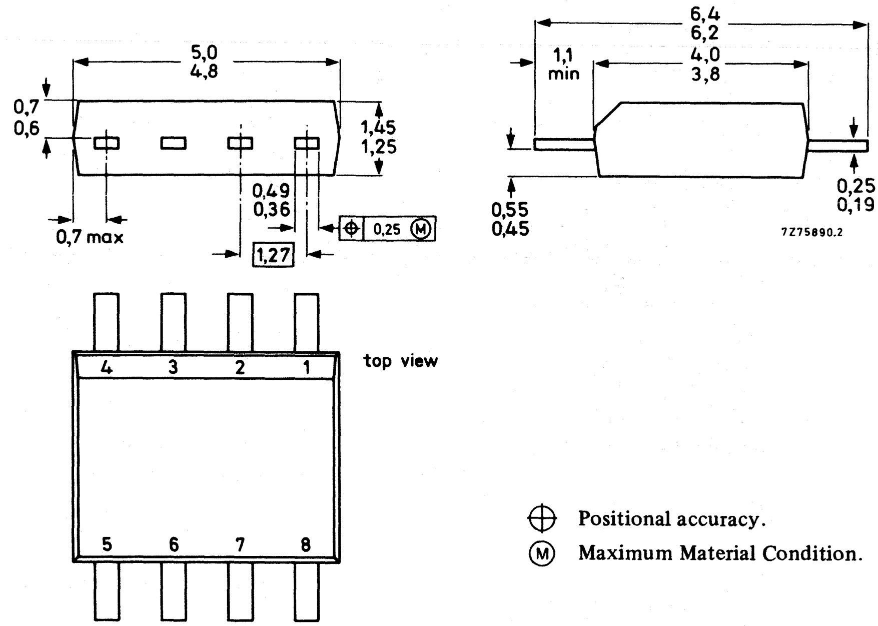
Table 3 Bonding pad locations (dimensions in μm)
All x/y co-ordinates are referenced to the bottom left pad (V_{DD}), see Fig.8.

pad	X	Y	pad	X	Y
S1	1490	881	G4/D4	–86	1588
DATA	1490	639	F4/E4	–86	1808
OSC IN	1490	408	B3/C3	–86	2028
OSC OUT	1490	188	G3/AD3	–86	2248
V_{SS}	1352	0	F3/E3	–48	2476
MODE	969	0	A4/COL	352	2476
V_{PP}	770	0	B2/C2	552	2476
TS	506	0	G2/D2	752	2476
ENABLE	306	0	F2/E2	952	2476
V_{DD}	0	0	B1/C1	1352	2476
FLASH	–86	188	A2/ADEG1	1490	2248
SEL	–86	408	AM/PM	1490	2028
S2	–86	628	BP2	1490	1808
B4/C4	–86	848	BP1	1490	1588
chip corner (max.)	–250	–160			

PACKAGE INFORMATION

Package outlines
Soldering

8-LEAD MINI-PACK; PLASTIC (SO8; SOT96C)

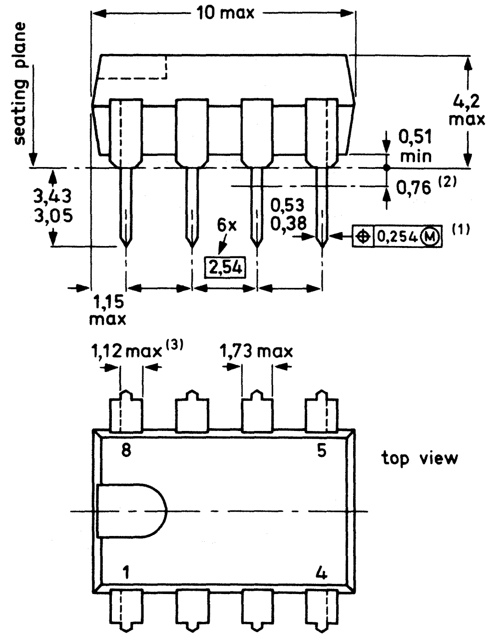


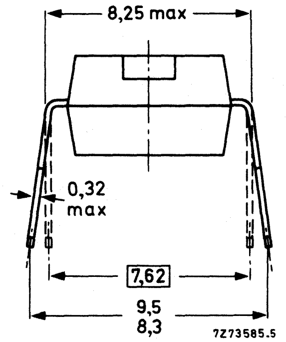
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

8-LEAD DUAL IN-LINE; PLASTIC (SOT97)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

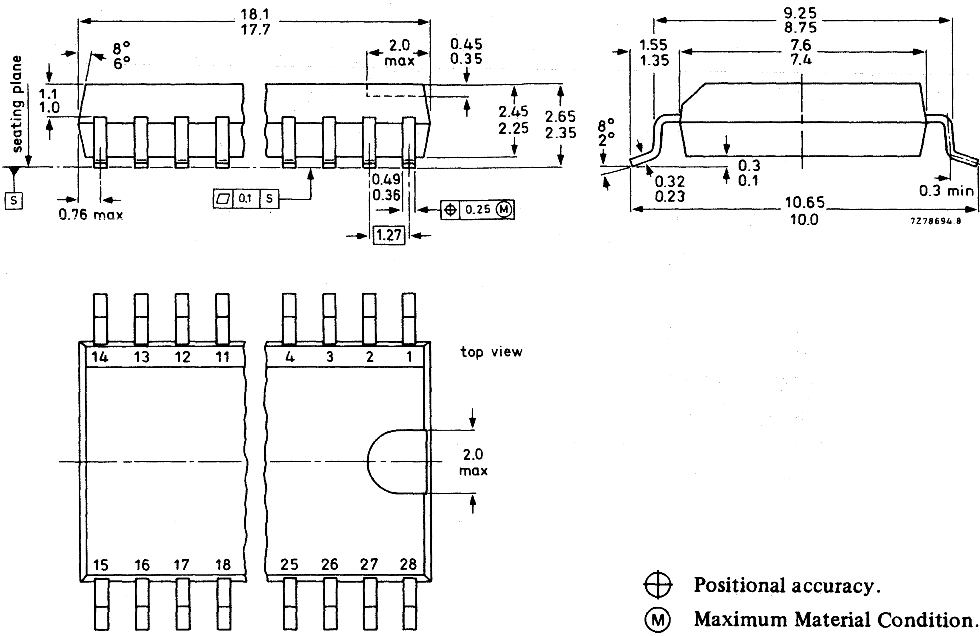
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

Dimensions in mm

28-LEAD MINI-PACK; PLASTIC (SO28; SOT136A)

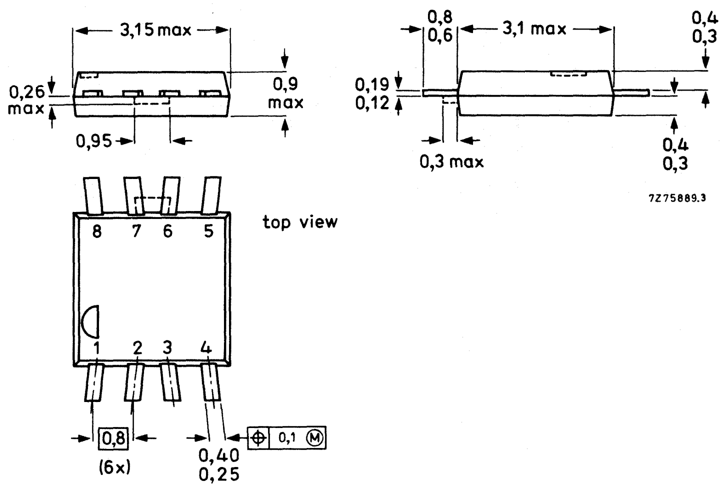


⊕ Positional accuracy.

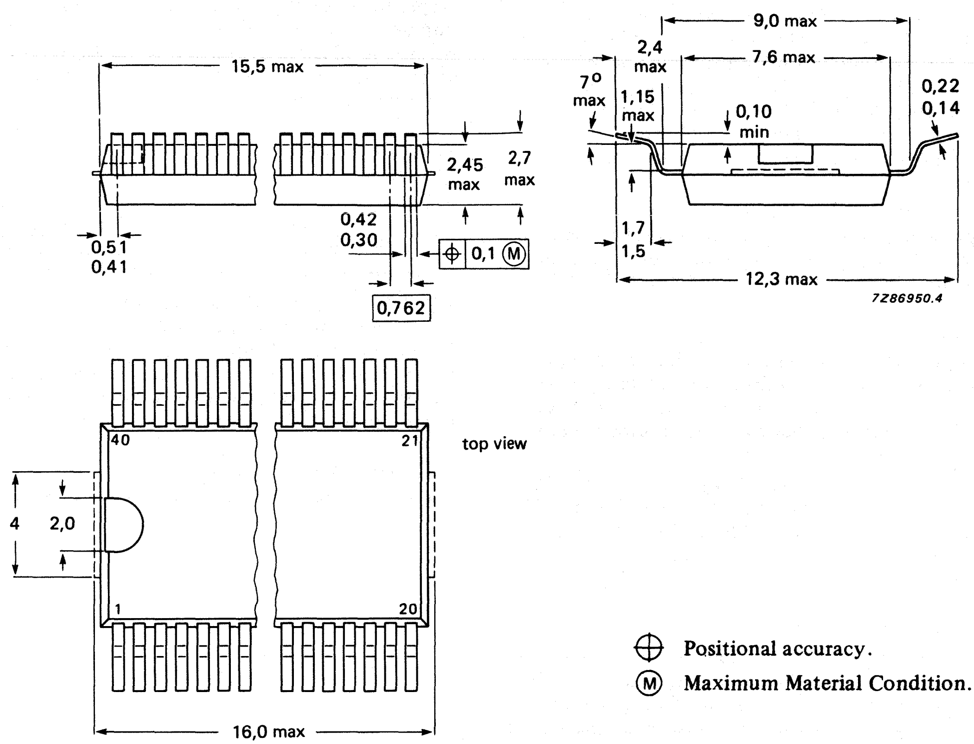
Ⓜ Maximum Material Condition.

Dimensions in mm

8-LEAD MICRO FLAT-PACK; PLASTIC (SOT144)



40-LEAD MINI-PACK; PLASTIC (OPPOSITE BENT LEADS) (VSO40; SOT158B)



Dimensions in mm

SOLDERING PLASTIC MINI-PACKS

1. By hand-held soldering iron or pulse-heated solder tool

Fix the component by first soldering two, diagonally opposite end leads. Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to substrate by dipping or by an extra thick tin/lead plating before package placement.

2. By wave

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

3. By solder paste reflow

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.

Pre-heating is necessary to dry paste and evaporate binding agent.

Pre-heating duration: 45 minutes at 45 °C.

4. Repairing soldered joints

The same precaution and limits apply as in (1) above.

SOLDERING PLASTIC DUAL IN-LINE PACKAGES

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

DATA HANDBOOK SYSTEM

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of six series of handbooks:

INTEGRATED CIRCUITS

DISCRETE SEMICONDUCTORS

DISPLAY COMPONENTS

PASSIVE COMPONENTS*

PROFESSIONAL COMPONENTS**

MATERIALS*

The contents of each series are listed on pages iii to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Components is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.
Product specialists are at your service and enquiries will be answered promptly.

* Will replace the Components and materials (green) series of handbooks.
** Will replace the Electron tubes (blue) series of handbooks.

INTEGRATED CIRCUITS

This series of handbooks comprises:

code	handbook title
IC01	**Radio, audio and associated systems** Bipolar, MOS
IC02a/b	**Video and associated systems** Bipolar, MOS
IC03	**ICs for Telecom** Bipolar, MOS Subscriber sets, Cordless Telephones
IC04	**HE4000B logic family** CMOS
IC05	**not yet issued**
IC06	**High-speed CMOS; PC74HC/HCT/HCU** Logic family
IC07	**Advanced CMOS logic (ACL)**
IC08	**ECL 10K and 100K logic families**
IC09N	**TTL logic series**
IC10	**Memories** MOS, TTL, ECL
IC11	**Linear Products**
Supplement to IC11	**Linear Products**
IC12	**I^2C-bus compatible ICs**
IC13	**Semi-custom** Programmable Logic Devices (PLD)
IC14	**Microcontrollers** NMOS, CMOS
IC15	**FAST TTL logic series**
IC16	**CMOS integrated circuits for clocks and watches**
IC17	**ICs for Telecom** Bipolar, MOS Radio pagers Mobile telephones ISDN
IC18	**Microprocessors and peripherals**
IC19	**Data communication products**

DISCRETE SEMICONDUCTORS

This series of data handbooks comprises:

current code	new code	handbook title
S1	**SC01**	**Diodes** High-voltage tripler units
S2a	**SC02***	**Power diodes**
S2b	**SC03***	**Thyristors and triacs**
S3	**SC04***	**Small-signal transistors**
S4a	**SC05**	**Low-frequency power transistors and hybrid IC power modules**
S4b	**SC06**	**High-voltage and switching power transistors**
S5	**SC07***	**Small-signal field-effect transistors**
S6	**SC08*** **SC09**	**RF power transistors** **RF power modules**
S7	**SC10**	**Surface mounted semiconductors**
S8a	**SC11***	**Light emitting diodes**
S8b	**SC12**	**Optocouplers**
S9	**SC13***	**PowerMOS transistors**
S10	**SC14***	**Wideband transistors and wideband hybrid IC modules**
S11	**SC15**	**Microwave transistors**
S15**	**SC16**	**Laser diodes**
S13	**SC17**	**Semiconductor sensors**
S14	**SC18***	**Liquid crystal displays and driver ICs for LCDs**

* Not yet issued with the new code in this series of handbooks.
** New handbook in this series; will be issued shortly.

DISPLAY COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
T8	**DC01**	**Colour display systems**
T16	**DC02**	**Monochrome tubes and deflection units**
C2	**DC03***	**Television tuners, coaxial aerial input assemblies**
C3	**DC04***	**Loudspeakers**
C20	**DC05***	**Wire-wound components for TVs and monitors**

* These handbooks are currently issued in another series; they are not yet issued in the Display Components series of handbooks.

PASSIVE COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
C14	**PA01**	**Electrolytic capacitors; solid and non-solid**
C11	**PA02***	**Varistors, thermistors and sensors**
C12	**PA03***	**Potentiometers, encoders and switches**
C7	**PA04***	**Variable capacitors**
C22	**PA05***	**Film capacitors**
C15	**PA06***	**Ceramic capacitors**
C9	**PA07***	**Piezoelectric quartz devices**
C13	**PA08***	**Fixed resistors**

* Not yet issued with the new code in this series of handbooks.

PROFESSIONAL COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
T1	*	Power tubes for RF heating and communications
T2a	*	Transmitting tubes for communications, glass types
T2b	*	Transmitting tubes for communications, ceramic types
T3	PC01**	High-power klystrons
T4	*	Magnetrons for microwave heating
T5	PC02**	Cathode-ray tubes
T6	PC03**	Geiger-Müller tubes
T9	PC04**	Photo and electron multipliers
T10	PC05**	Plumbicon camera tubes and accessories
T11	PC06	Microwave diodes and sub-assemblies
T12	PC07	Vidicon and Newvicon camera tubes and deflection units
T13	PC08	Image intensifiers
T15	PC09**	Dry reed switches
C8	PC10	Variable mains transformers; annular fixed transformers
	PC11	Solid state image sensors and peripheral integrated circuits

* These handbooks will not be reissued.

** Not yet issued with the new code in this series of handbooks.

MATERIALS

This series of data handbooks comprises:

current code	new code	handbook title
C4 **C5**	**MA01***	**Soft Ferrites**
C16	**MA02****	**Permanent magnet materials**
C19	**MA03****	**Piezoelectric ceramics**

* Handbooks C4 and C5 will be reissued as one handbook having the new code MA01.

** Not yet issued with the new code in this series of handbooks.

Philips Components – a worldwide Group of Companies

Argentina: PHILIPS ARGENTINA S.A., Div. Philips Components, Vedia 3892, 1430 BUENOS AIRES, Tel. (01) 541 -4261.
Australia: PHILIPS COMPONENTS PTY Ltd, 11 Waltham Street, ARTARMON, N.S.W. 2064, Tel. (02)439 3322.
Austria: ÖSTERREICHISCHE PHILIPS INDUSTRIE G.m.b.H., UB Bauelemente, Triester Str. 64, 1101 WIEN, Tel. (0222) 60 101-820.
Belgium: N.V. PHILIPS PROF. SYSTEMS – Components Div., 80 Rue Des Deux Gares, B-1070 BRUXELLES, Tel. (02) 52 56 111.
Brazil: PHILIPS COMPONENTS (Active Devices): Av. Brigadeiro Faria Lima, 1735-SAO PAULO-SP, Tel. (011) 211-2600. PHILIPS COMPONENTS (Passive Devices & Materials): Av. Francisco Monteiro, 702-RIBEIRO PIRES-SP, Tel. (011) 459-8211.
Canada:
Chile: PHILIPS CHILENA S.A., Av. Santa Maria 0760, SANTIAGO, Tel. (02) 77 38 16.
Colombia: IPRELENSO LTDA., Carrera 21 No. 56-17, BOGOTA, D.E., P.O. Box 77621, Tel. (01) 249 76 24.
Denmark: PHILIPS COMPONENTS A/S, Prags Boulevard 80, PB1919, DK-2300 COPENHAGEN S, Tel. 01-54 11 33.
Finland: PHILIPS COMPONENTS, Sinikalliontie 3, SF-2630 ESPOO HELSINKI 10, Tel. 358-0-50 261.
France: PHILIPS COMPOSANTS RTC-COMPELEC, 117 Quai du Président Roosevelt, 92134 ISSY-LES-MOULINEAUX Cedex, Tel. (01) 40 93 80 00.
Germany (Fed. Republic): VALVO, UB Bauelemente der Philips G.m.b.H., Valvo Haus, Burchardstrasse 19, D-2 HAMBURG 1, Tel. (040) 3296-0.
Greece: PHILIPS HELLENIQUE S.A., Components Division, No. 15, 25th March Street, GR 17778 TAVROS, Tel. (01) 4894 339/4894 911.
Hong Kong: PHILIPS HONG KONG LTD., Components Div., 15/F Philips Ind. Bldg., 24-28 Kung Yip St., KWAI CHUNG, Tel. (0)-24 51 21.
India: PEICO ELECTRONICS & ELECTRICALS LTD., Components Dept., Band Box Building, 254-D Dr. Annie Besant Rd., BOMBAY – 400 025, Tel. (022) 4930311/4930590.
Indonesia: P.T. PHILIPS-RALIN ELECTRONICS, Components Div., Setiabudi II Building, 6th Fl., Jalan H.R. Rasuna Said (P.O. Box 223/KBY) Kuningan, JAKARTA 12910, Tel. (021) 51 79 95.
Ireland: PHILIPS ELECTRONICS (IRELAND) LTD., Components Division, Newstead, Clonskeagh, DUBLIN 14, Tel. (01) 69 33 55.
Italy: PHILIPS S.p.A., Philips Components, Piazza IV Novembre 3, I-20124 MILANO, Tel. (02) 6752.1.
Japan: PHILIPS K.K. Philips Components Division, Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO (108), Tel. (03) 740 5028.
Korea (Republic of): PHILIPS ELECTRONICS (KOREA) LTD. Components Division, Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL, Tel. (02) 794-5011.
Malaysia: PHILIPS MALAYSIA SDN BHD, Components Div., 3 Jalan SS15/2A SUBANG, 47500 PETALING JAYA, Tel. (03) 73 45 511.
Mexico: PHILIPS COMPONENTS, Paseo Triunfo de la Republica, No 215 Local 5,Cd Juarez CHIHAUHAU 32340 MEXICO Tel.(16) 18-67-01/02
Netherlands: PHILIPS NEDERLAND, Marktgroep Philips Components, Postbus 90050, 5600 PB EINDHOVEN, Tel. (040) 78 37 49.
New Zealand: PHILIPS NEW ZEALAND LTD., Components Division, 110 Mt. Eden Road, C.P.O. Box 1041, AUCKLAND, Tel. (09) 605-914.
Norway: NORSK A/S PHILIPS, Philips Components, Box 1, Manglerud 0612, OSLO, Tel. (02) 68 02 00.
Pakistan: PHILIPS ELECTRICAL CO. OF PAKISTAN LTD., Philips Markaz, M.A. Jinnah Rd., KARACHI-3, Tel. (021) 72 57 72.
Peru: CADESA, Av. Pardo y Aliaga No. 695, 6th Floor, San Isidro, LIMA 100, P.O. Box 5612, Tel. (014) 70 70 80.
Philippines: PHILIPS INDUSTRIAL DEV. INC., 2246 Pasong Tamo, P.O. Box 911, Makati Comm. Centre, MAKATI-RIZAL 3116, Tel. (02) 86 89 51 to 59.
Portugal: PHILIPS PORTUGUESA S.A.R.L., Av. Eng. Duarte Pacheco 6, 1009 LISBOA Codex, Tel. (019) 68 31 21.
Singapore: PHILIPS PROJECT DEV. (Singapore) PTE LTD., Components Div., Lorong 1, Toa Payoh, SINGAPORE 1231, Tel. 35 02 000.
Spain: PHILIPS Components, Balmes 22, 08007 BARCELONA, Tel. (03) 301 63 12.
Sweden: PHILIPS Components, A.B., Tegeluddsvägen 1, S-11584 STOCKHOLM, Tel. (0)8-78 21 000.
Switzerland: PHILIPS A.G., Components Dept., Allmendstrasse 140-142, CH-8027 ZÜRICH, Tel. (01) 488 22 11.
Taiwan: PHILIPS TAIWAN LTD., 150 Tun Hua North Road, P.O. Box 22978, TAIPEI, Taiwan, Tel. (02) 71 20 500.
Thailand: PHILIPS ELECTRICAL CO. OF THAILAND LTD., 283 Silom Road, P.O. Box 961, BANGKOK, Tel. (02) 233-6330-9.
Turkey: TÜRK PHILIPS TICARET A.S., Philips Components,Talatpasa Cad. No. 5, 80640 LEVENT/ISTANBUL, Tel. (01) 179 27 70.
United Kingdom: PHILIPS COMPONENTS LTD., Mullard House, Torrington Place, LONDON WC1E 7HD, Tel. (01) 580 6633.
United States: (Active Devices & Materials) AMPEREX Electronic Corporation, Providence Pike, SLATERSVILLE, R.I. 02876, Tel. (401) 762-9000. (Colour picture tubes – Monochrome & Colour Display Tubes) PHILIPS DISPLAY COMPONENTS, 50 Johnston St., SENECA FALLS, N.Y. 13148, Tel. (315) 568-5881. (IC Products) SIGNETICS CORPORATION, 811 East Arques Avenue, SUNNYVALE, CA 94088-3409, Tel. (408) 991-2000. (Passive & Electromech. Dev.) MEPCO/CENTRALAB, INC., 2001 West Blue Heron Blvd, RIVIERA BEACH, Florida 33404, P.O. Box 10330, Tel. (407) 881-3200.
Uruguay: PHILIPS COMPONENTS, Coronel Mora 433, MONTEVIDEO, Tel. (02)70-4044.
Venezuela: MAGNETICA S.A., Calle 6, Ed. Las Tres Jotas, CARACAS 1074A, App. Post. 78117, Tel. (02) 241 75 09.
Zimbabwe: PHILIPS ELECTRICAL (PVT) LTD., 62 Mutare Road, HARARE, P.O. Box 994, Tel. 47211

For all other countries apply to: Philips Components Division, International Business Relations, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Telex 35000 phtcnl

AS69 © Philips Export B.V. 1989

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands 9398 153 50011

Philips Components

PHILIPS

PHILIPS